

MODEL NAME : AAP01
PROJECT CODE : ANRAAP0100
PCB NO :
DAA000AK000 LA-C901P M/B
DA400237000 LS-C901P SSD/B
DA40023X000 LS-C902P SSD/B (w/o redriver)
DA40023Y000 LS-C904P LOGO/B

ZZZ PCB@
PCB 1FU LA-C901P REV0 M/B MLK 3
DAA000AK000

ZZZ PCBR1@
PCB 1FU LA-C901P REV1 M/B MLK 3
DAA000AK010


ZZZ PCBR3@
PCB 1FU LA-C901P REV1 MB MLK TRIP 3 A31!
DAA000AK011

ZZZ DAZR1@
PCB AAP01 LA-C901P LS-A302P/A303P/C904P 02
DAZ1FU00100

ZZZ DAZR3@
PCB AAP01 LA-C901P LS-A302P/A303P/C904P 02 TRIPOD A31 !
DAZ1FU00101

HDMI@ ROYALTY HDMI W/LOGO	
Part Number	Description
80000000020M	HDMI W/Logo:80000000020M

Layout Dell logo



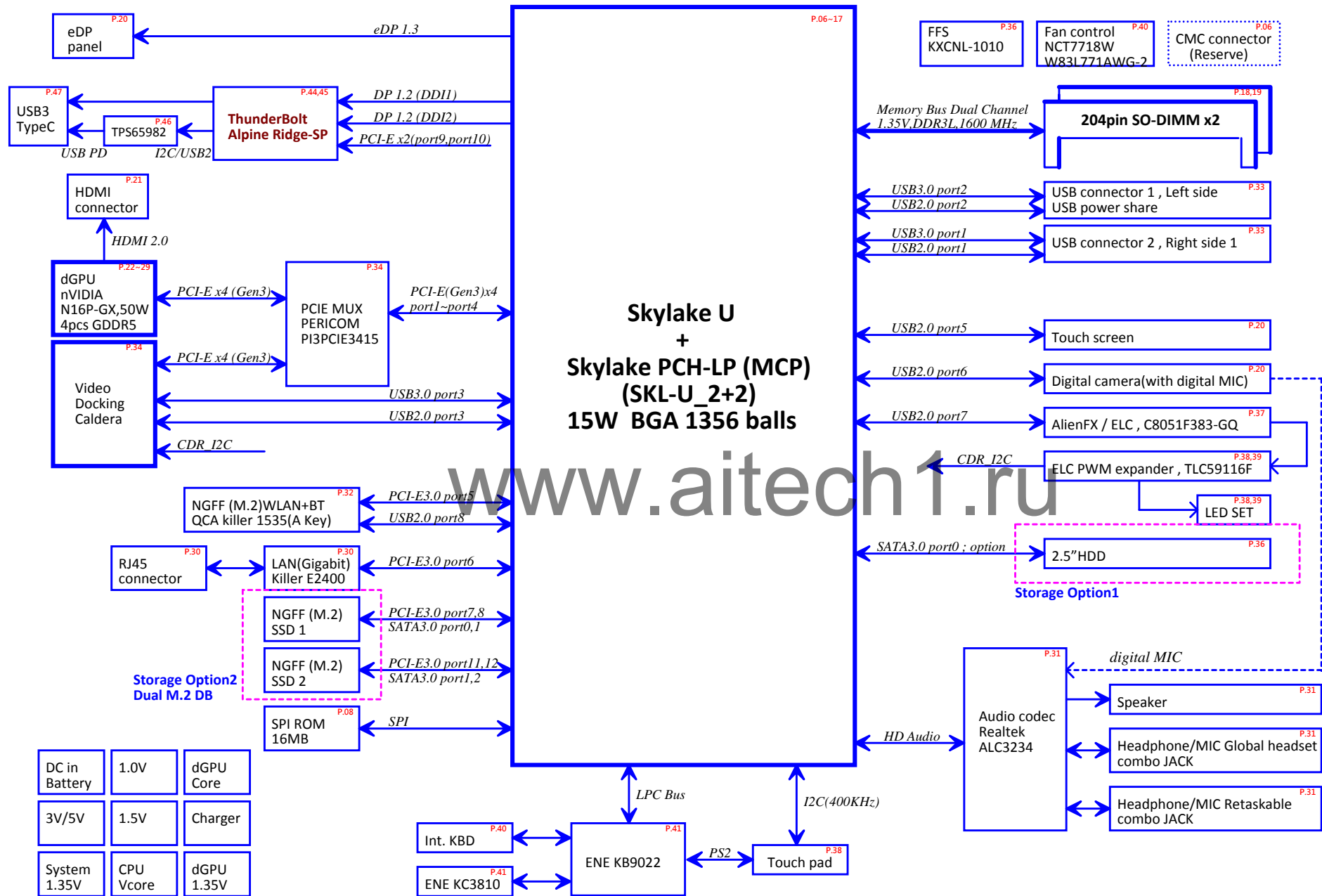
COPYRIGHT 2015
ALL RIGHT RESERVED
REV: X00
PWB: XXXXX
DATE: 1450-06

Echo MLK 13" SKL-U
Skylake U-type (1 chip_DSC)

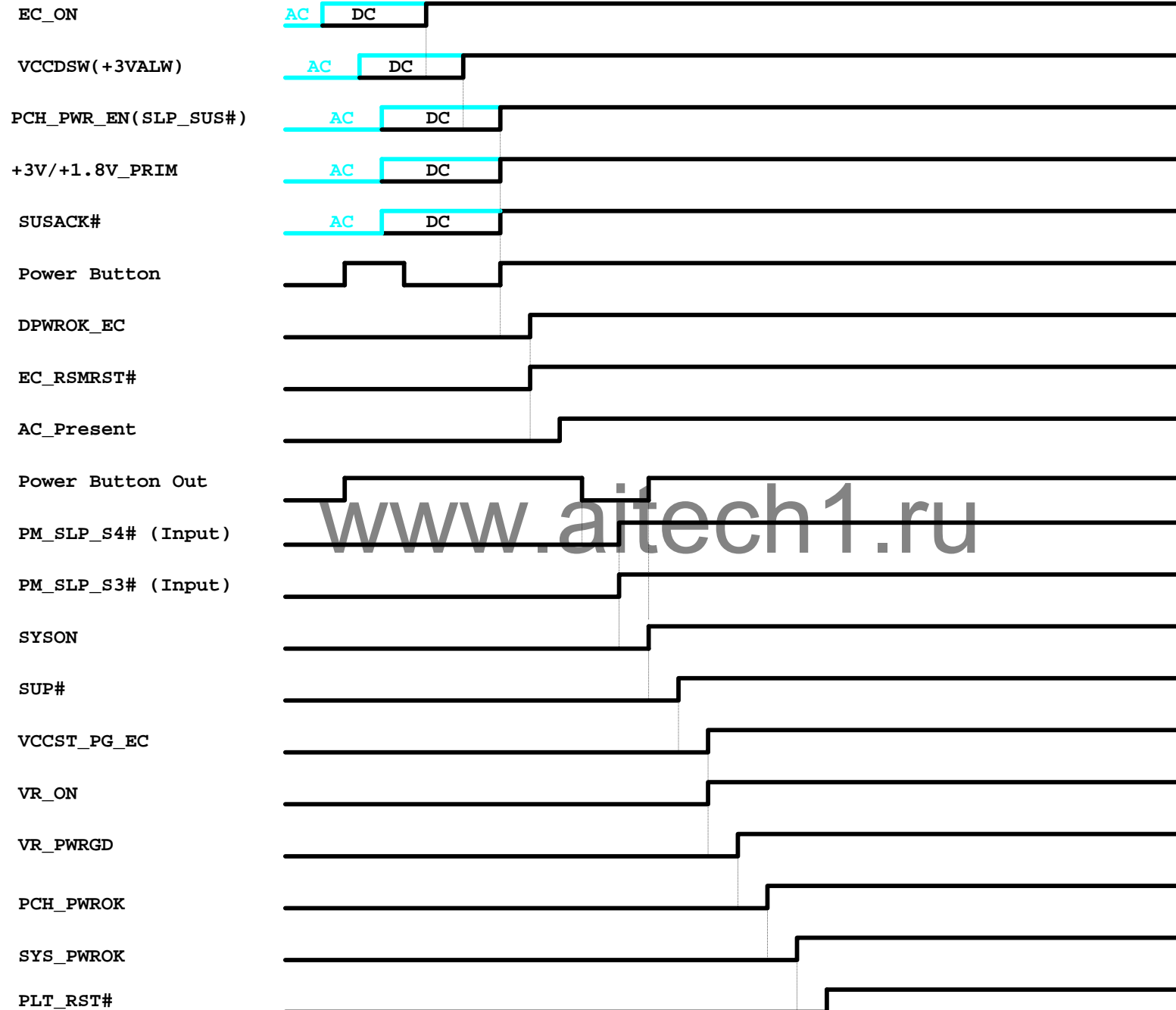
REV : 1.0 (A00)

2015.07.14

@ : Nopop Component
EMI@,ESD@ : EMI/ESD/RF part
CONN@ : Connector Component
CMC@ : Total debug Component



Power on sequence



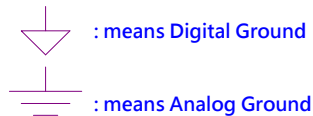
Board ID Table for AD channel

Vcc	3.3V				
Ra	100K +/- 1%				
Board ID	Rb	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max	EC AD3
0	0		0.000V	0.300V	0x00 - 0x13
1	12K +/- 1%	0.347V	0.354V	0.360V	0x14 - 0x1E
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1F - 0x25
3	20K +/- 1%	0.541V	0.550V	0.559V	0x26 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3A
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3B - 0x45
6	43K +/- 1%	0.978V	0.992V	1.006V	0x46 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA4
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA5 - 0xAF
13	240K +/- 1%	2.316V	2.329V	2.343V	0xB0 - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xBF
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC0 - 0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD4
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD5 - 0xDD
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDE - 0xF0
19	NC	3.000V	3.000V		0xF1 - 0xFF

Board ID table and PCB version

ID	Rb		
0	0	EVT(R0.1)	
1	12K	DVT-1(R0.2)	
2	15K	DVT-1.1(R0.3)	
3	20K	DVT-2(R0.4)	
4	27K	Pilot(R1.0)	
5	33K		
6	43K		
7	56K		

Symbol Note :



CLOCK SIGNAL

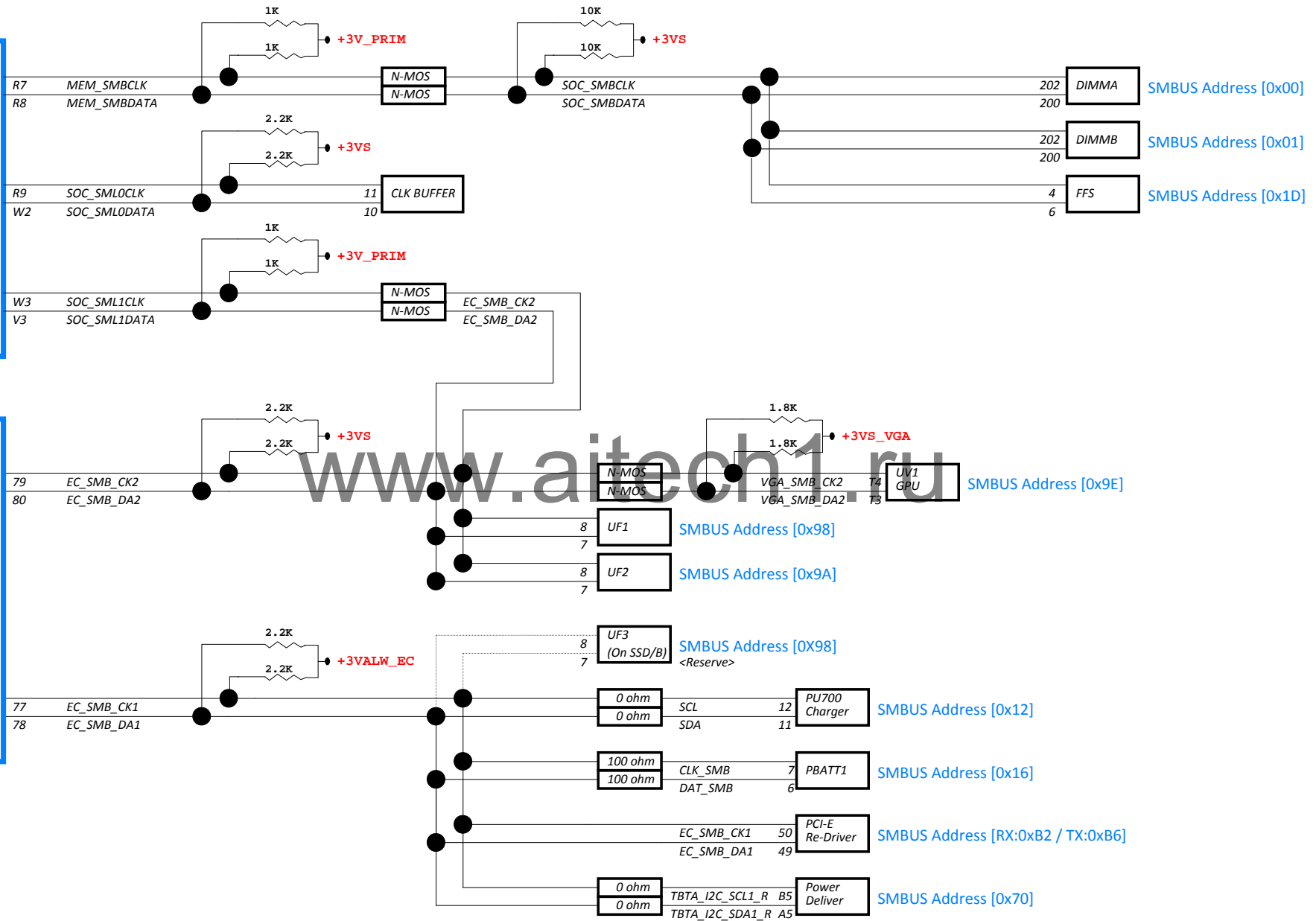
CLKOUT_PCIE0	N16P-GX +Caldera
CLKOUT_PCIE1	M.2 Card WLAN+BT
CLKOUT_PCIE2	Giga LAN
CLKOUT_PCIE3	M.2 NGFF SSD
CLKOUT_PCIE4	Thunderbolt
CLKOUT_PCIE5	M.2 NGFF SSD

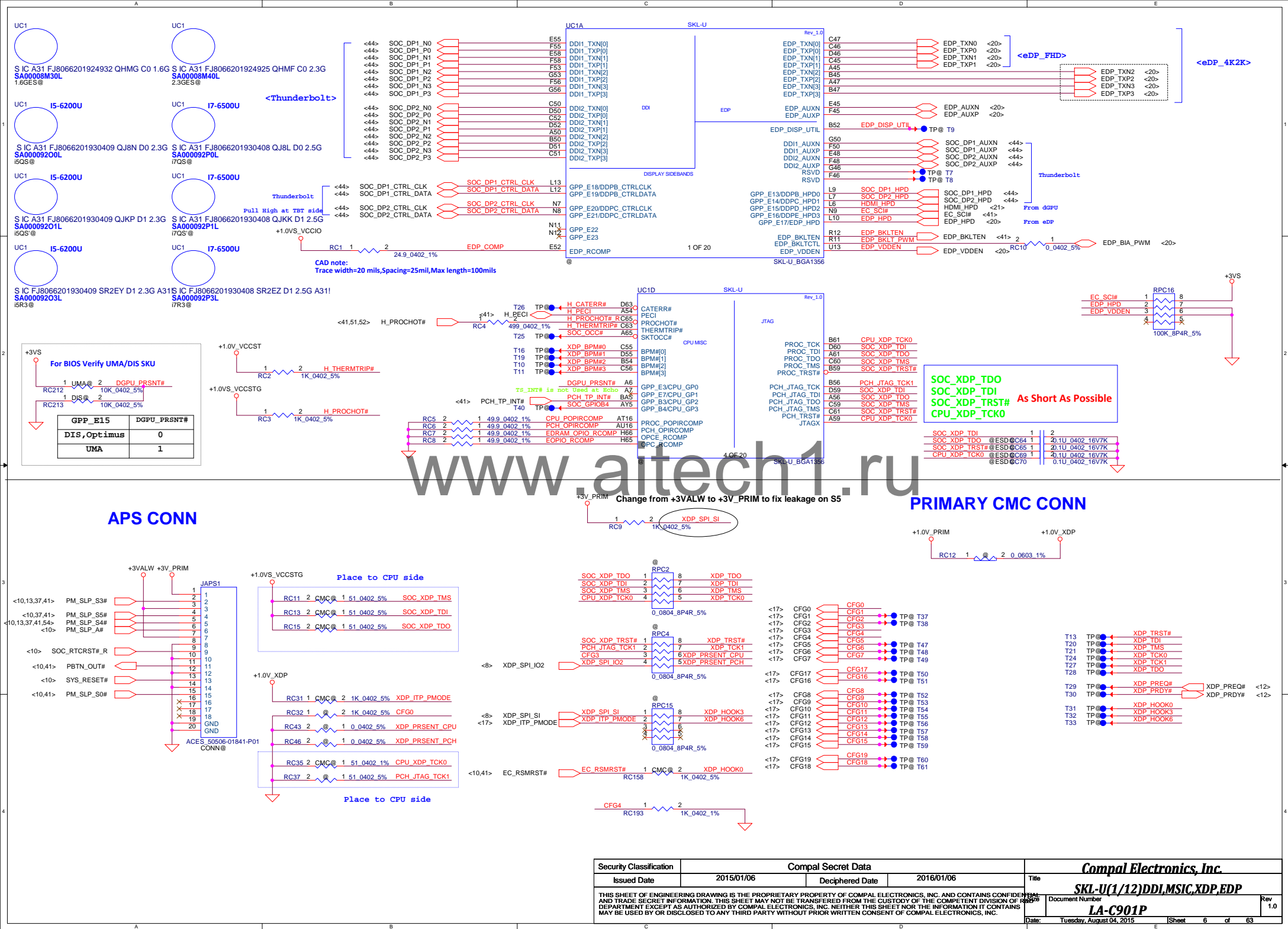
ULT

USB3.0	
Port1	Right side 1
Port2	Left side (power share)
Port3	Caldera
Port4	
USB2.0	
Port1	Right side 1
Port2	Left side (power share)
Port3	Caldera
Port4	
Port5	Touch screen
Port6	Camera
Port7	ELC
Port8	BT
PCI EXPRESS	
Lane 1~4	MUX for dGPU & Caldera
Lane 5	WLAN(M.2 Card)
Lane 6	10/100/1000 LAN
Lane 7~8	M.2 SATA+PCIeX2
Lane 9~10	Alpine Ridge SP
Lane 11~12	M.2 SATA+PCIeX2
SATA	
SATA0	HDD or SSD1
SATA1	SSD2
SATA2	SSD2
SATA3	

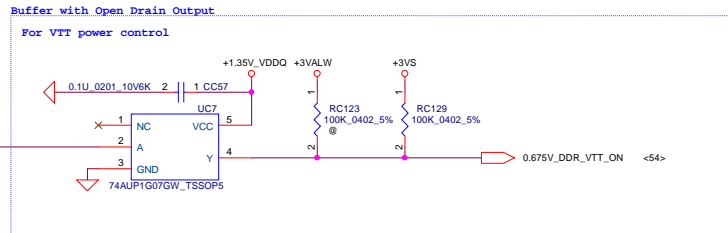
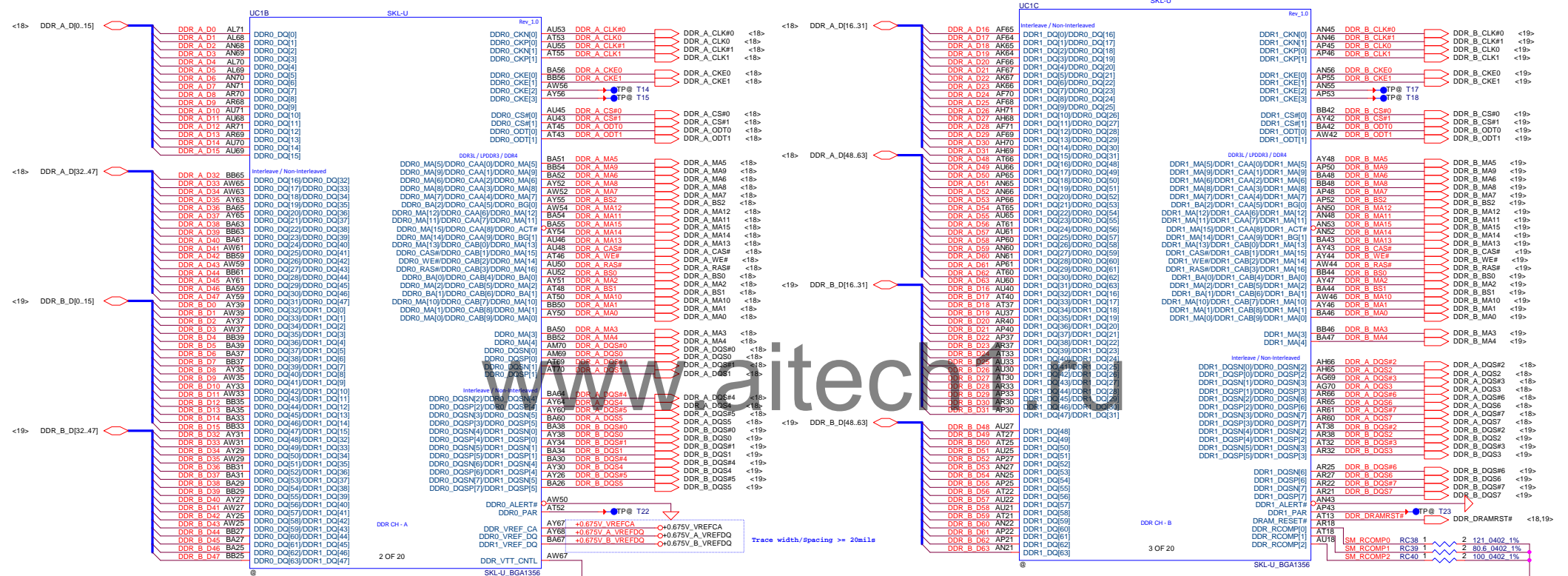
SKYLAKE
ULT

KBC
KB9022QD

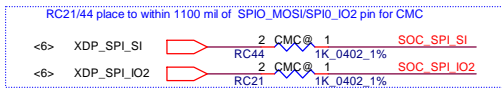




Non-Interleaved Memory



Security Classification		Compal Secret Data		Title	
Issued Date	2015/01/06	Deciphered Date	2016/01/06	Size	Document Number
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Date: Tuesday, August 04, 2015				Sheet	7 of 83



SOC_SMBALERT#

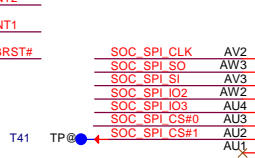
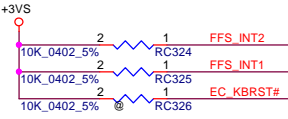
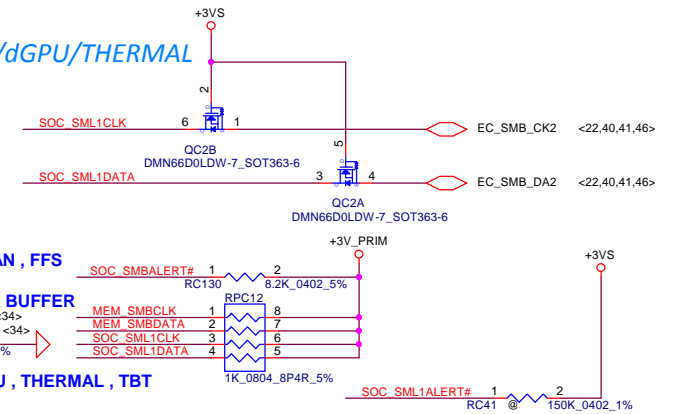
TLS CONFIDENTIALITY	
HIGH	ENABLE
LOW(DEFAULT)	DISABLE

SOC_SML0ALERT#

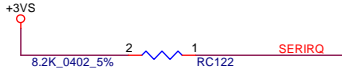
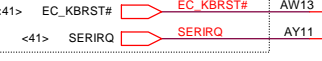
EC interface	
HIGH	ESPI
LOW(DEFAULT)	LPC

----->For KB9032 Only.
----->For KB9022/9032 Use

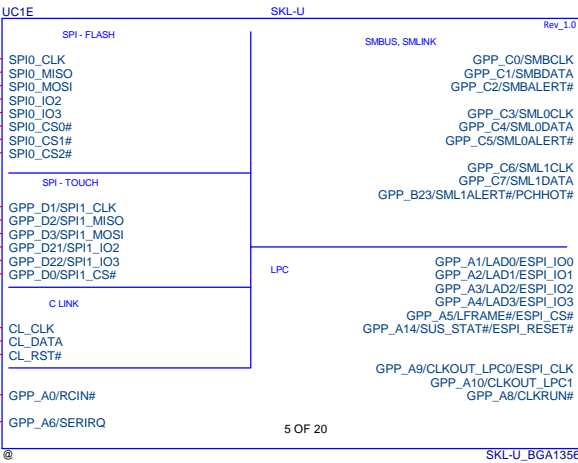
SML1 Bus : EC/dGPU/THERMAL



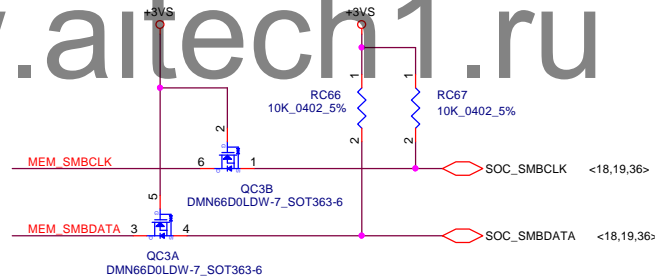
LPC Mode



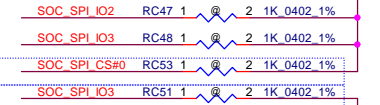
Follow 543016_SKL_U_Y_PDG_0_9



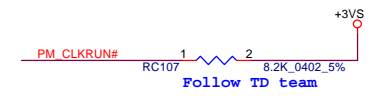
SMB Bus : DDR/WLAN/FFS



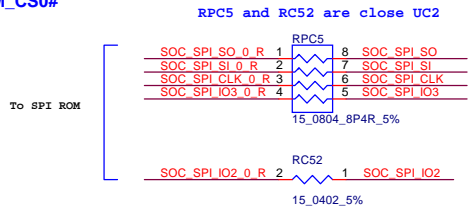
Reserve For EC Auto Load Code



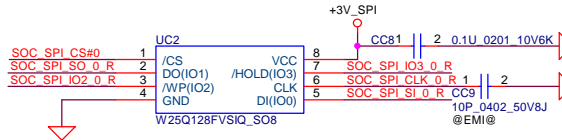
*****ONLY*****
From WW36 MOW for SKL-U ES sample



Single SPI ROM_CS0#



16M SPI ROM(Support ISH)



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				Rev	1.0
				Sheet	8 of 63

#545659 SKL_PCH_EDS_R0.7 P.84

11.7.3 Intel HD Audio link capabilities

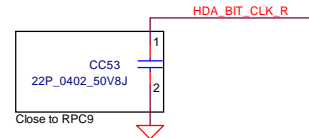
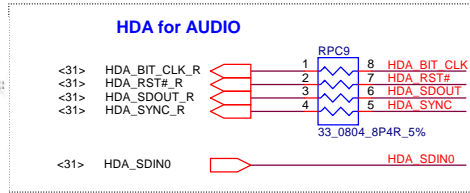
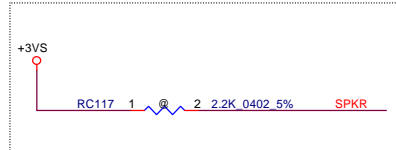
- Two SDI signals to support two external codecs.
- Drives variable frequency (6 MHz to 24 MHz) BCLK to support:
 - SDO double pumped up to 48 Mb/s
 - SDI's single pumped up to 24 Mb/s
- Provides cadence for 44.1 kHz-based sample rate output.
- Supports 1.5V, 1.8V and 3.3V modes.

Functional Strap Definitions

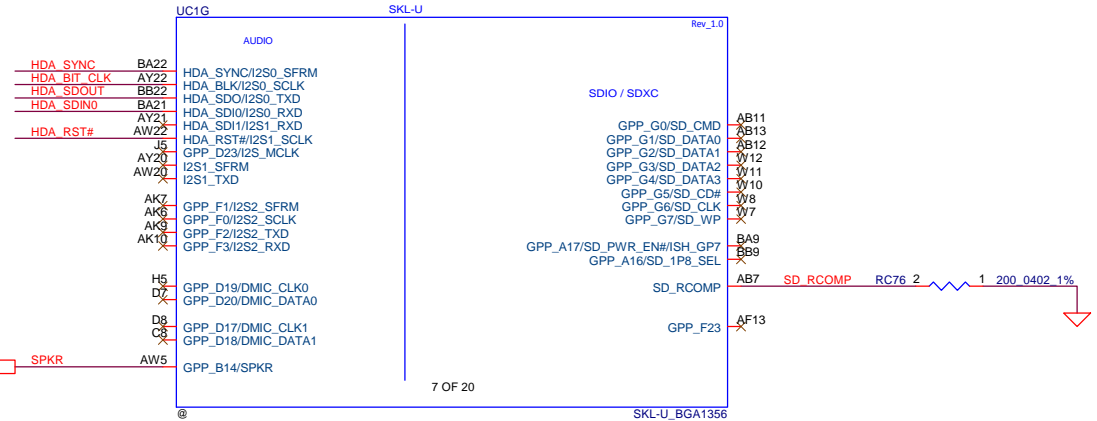
SPKR / GPP_B14 (Internal Pull Down):
(Sampled: Rising edge of PCH_PWROK)

TOP Swap Override
0 = Disable TOP Swap mode. --> AAX05 use
1 = Enable TOP Swap Mode.

TOP Swap Override



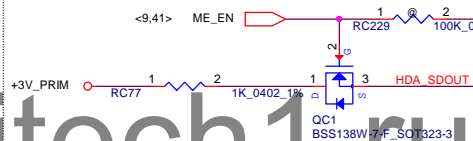
<31> SPKR



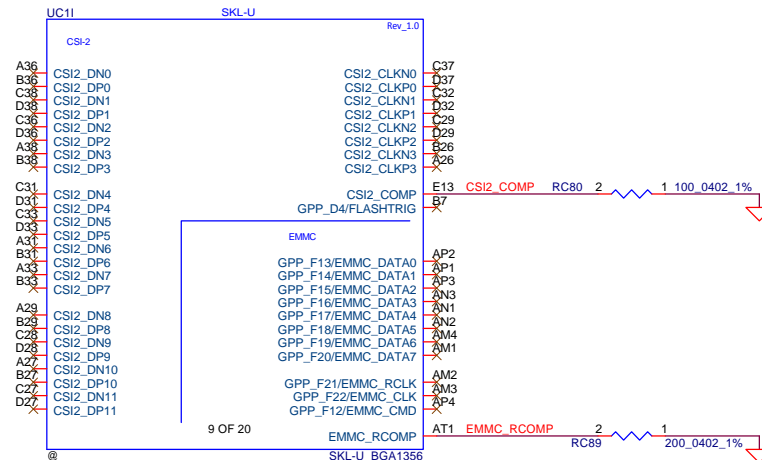
To Enable ME Override

Reserve RC229 follow TD team dat.04/23

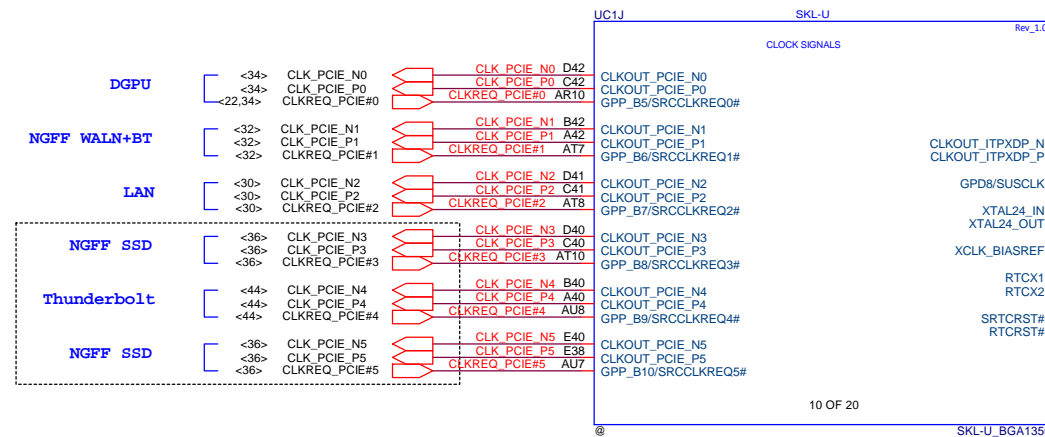
TD Team Solution



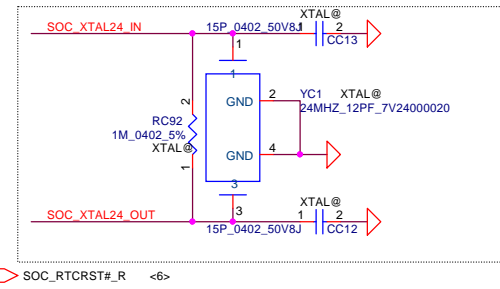
ABO Solution



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				Rev	1.0

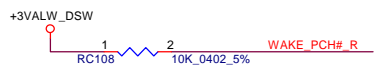
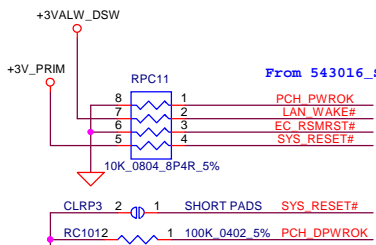
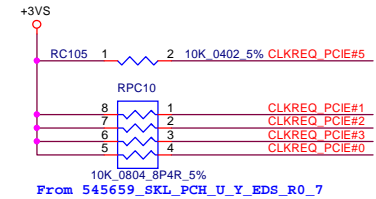
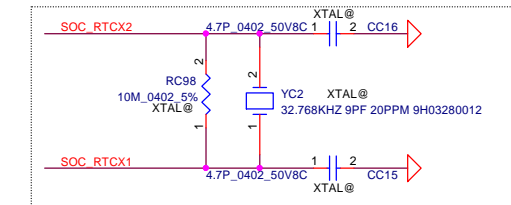


****Avoid Sub-trace****
Closed to CPU

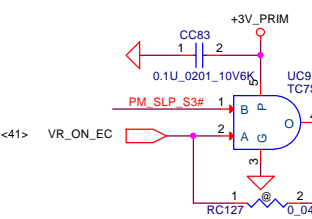
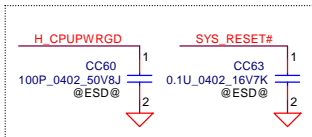


****Avoid Sub-trace****

Closed to CPU

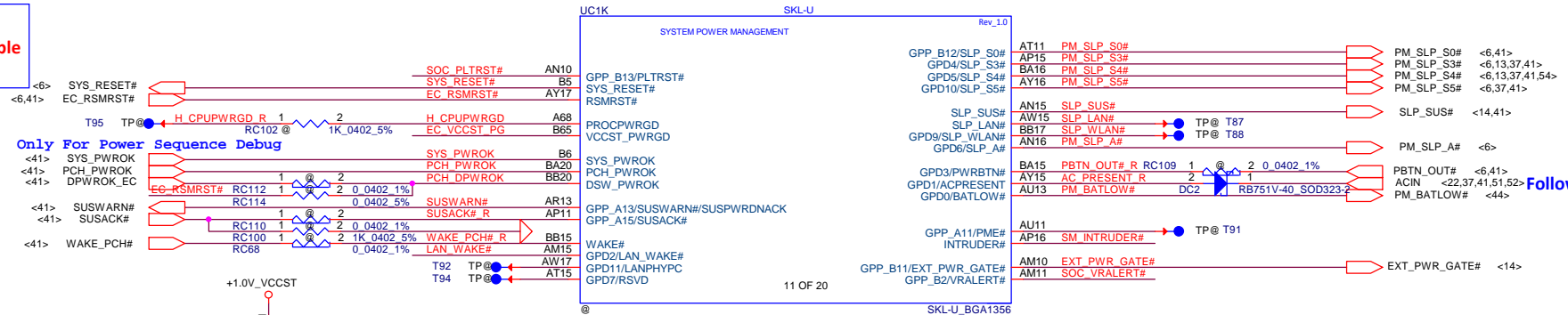
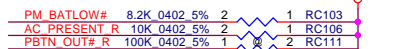
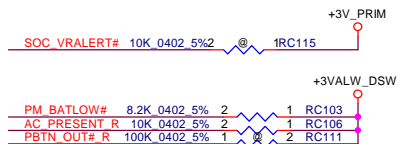
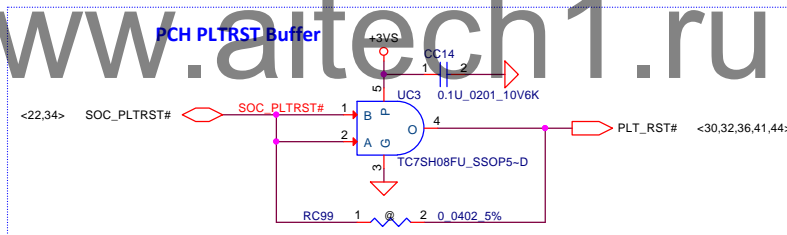


**EC_VCCST_PG
H_CPUWGRD As Short As Possible
SYS_RESET#**



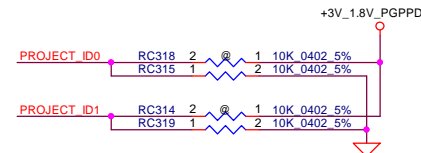
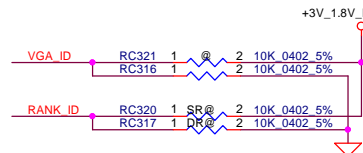
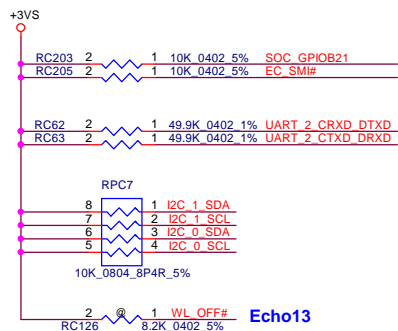
For meet tPLT17 & tCPU28 power down sequence.
tPLT17 : 1us (Max)
tCPU28 : 1us (Max)

www.aitech1.ru



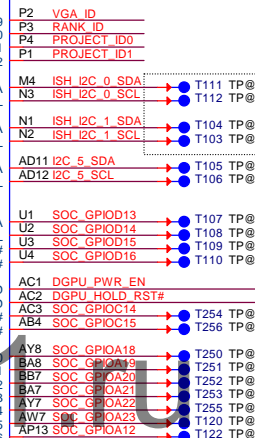
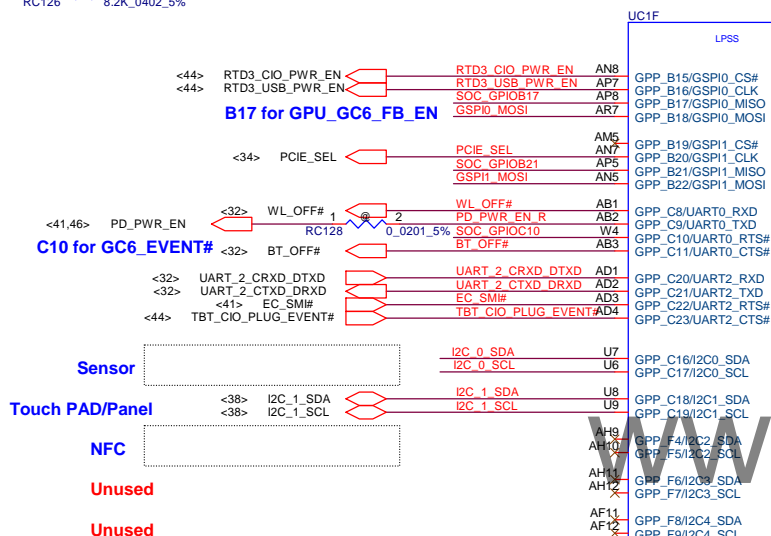
Follow Echo

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				SKL-U(5/12)CLK,GPIO	
				Size	Document Number
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				LA-C901P	
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VGA_ID	GPP_D9	RANK_ID	GPP_D10
GL	0	DR	0
GM	1	SR	1

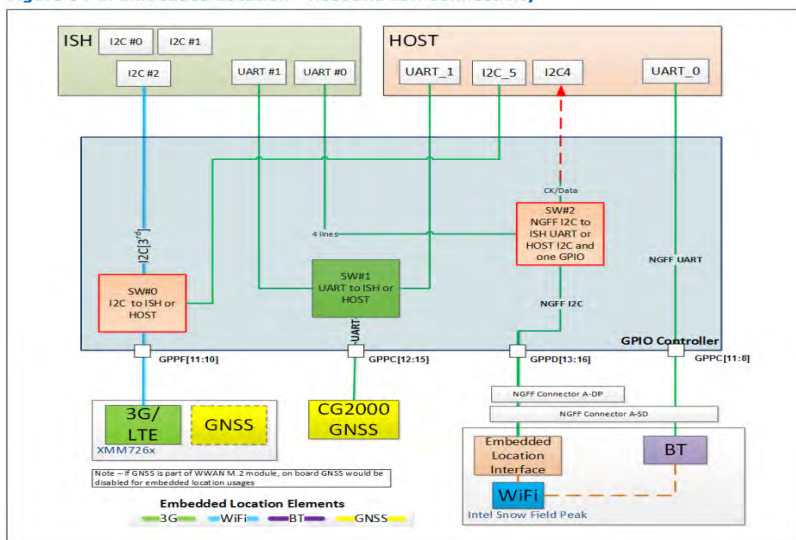
Project ID	Project_ID1 GPP_D12	Project_ID0 GPP_D11
*Project code	0	0
Reserved	0	1
Reserved	1	0
Reserved	1	1



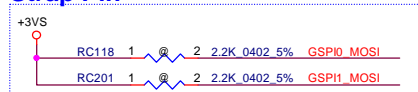
Unused

DGPU_PWR_EN <24>
DGPU_HOLD_RST# <22>

Figure 64-1. Embedded Location - Host and ISH Connectivity



Strap Pin



GSPI0_MOSI (Internal Pull Down):

No Reboot

0 = Disable No Reboot mode. --> AAX05 Use

1 = Enable No Reboot Mode. (PCH will disable the TCO Timer system reboot feature). This function is useful when running JTP/XDP.

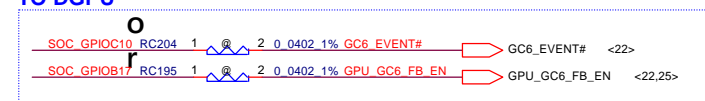
GSPI1_MOSI (Internal Pull Down):

Boot BIOS Strap Bit

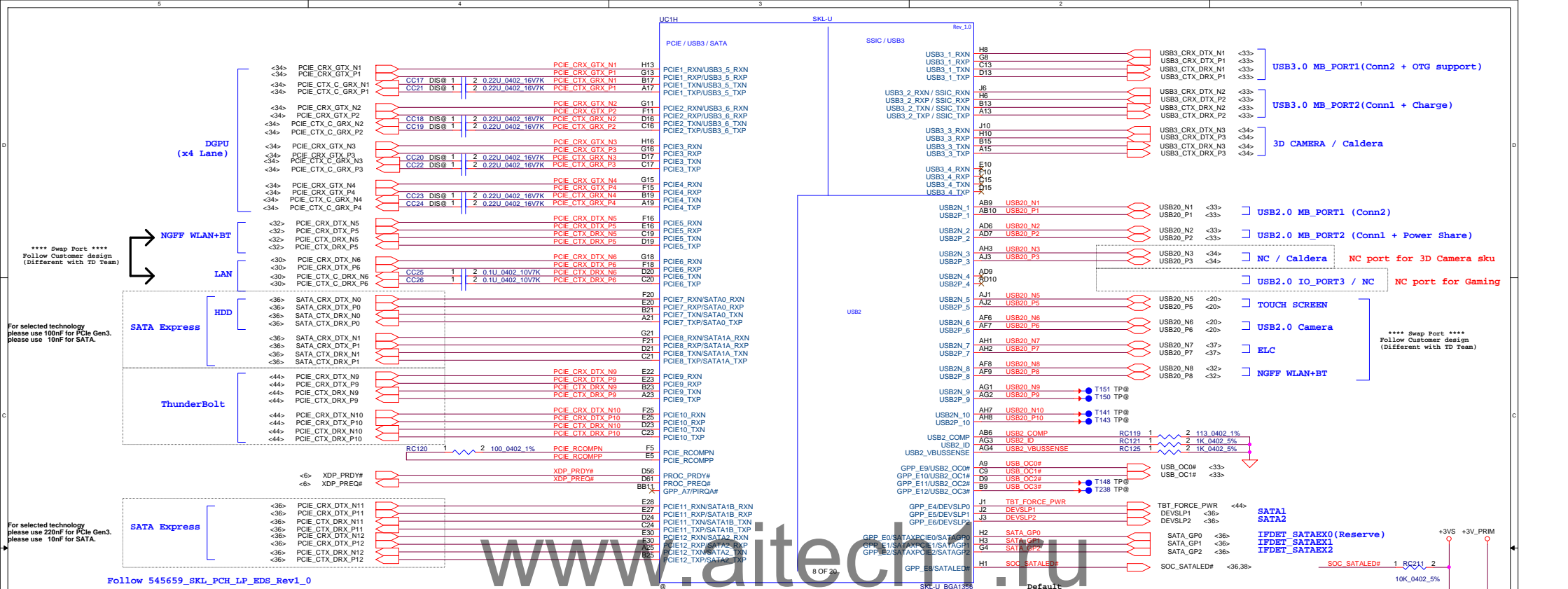
0 = SPI Mode --> AAX05 Use

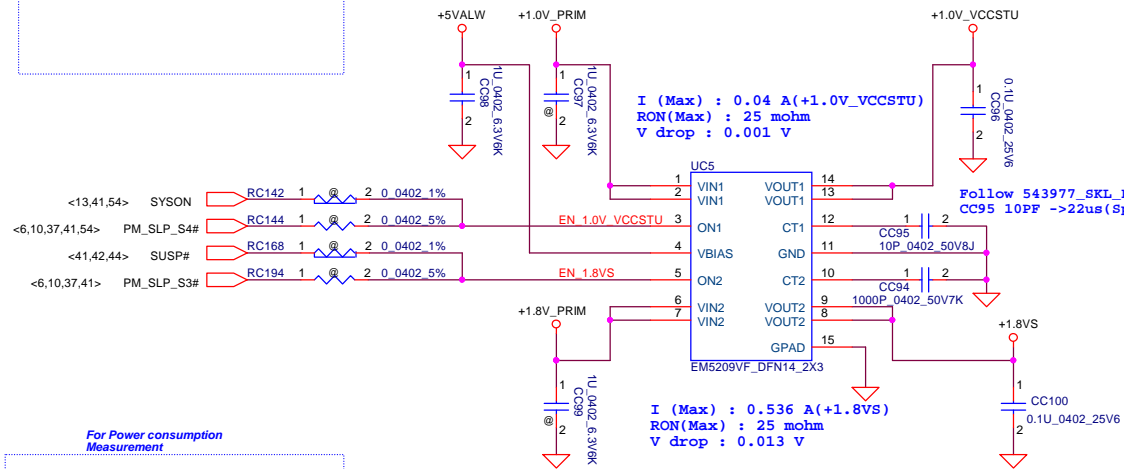
1 = LPC Mode--> AAP01 Use

TO DGPU F

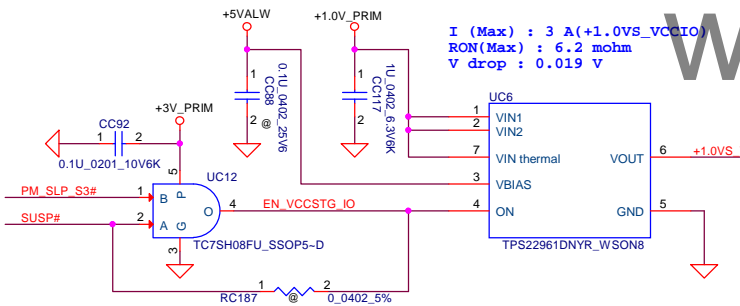


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Title			Compal Electronics, Inc.	
Size			SKL-U(6/12)GPIO	
Date			Tuesday, August 04, 2015	
Sheet			11 of 63	

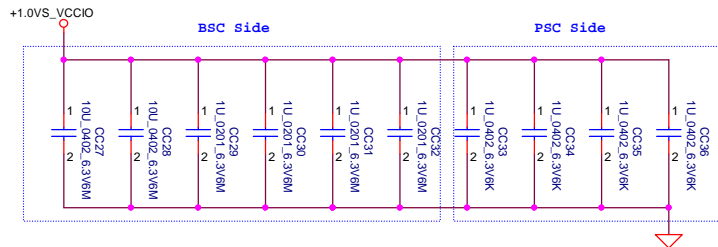




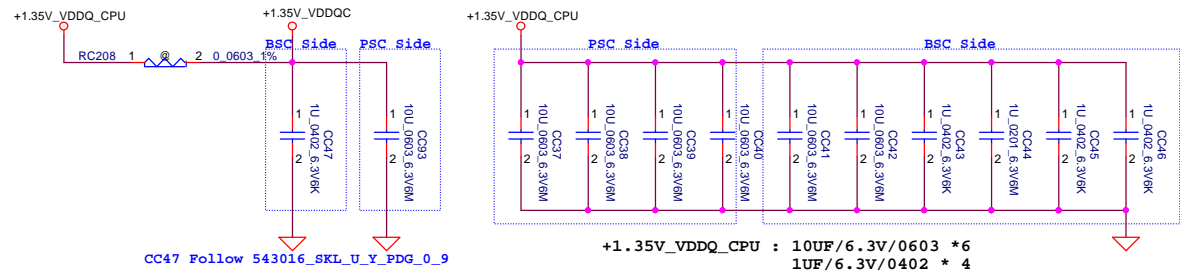
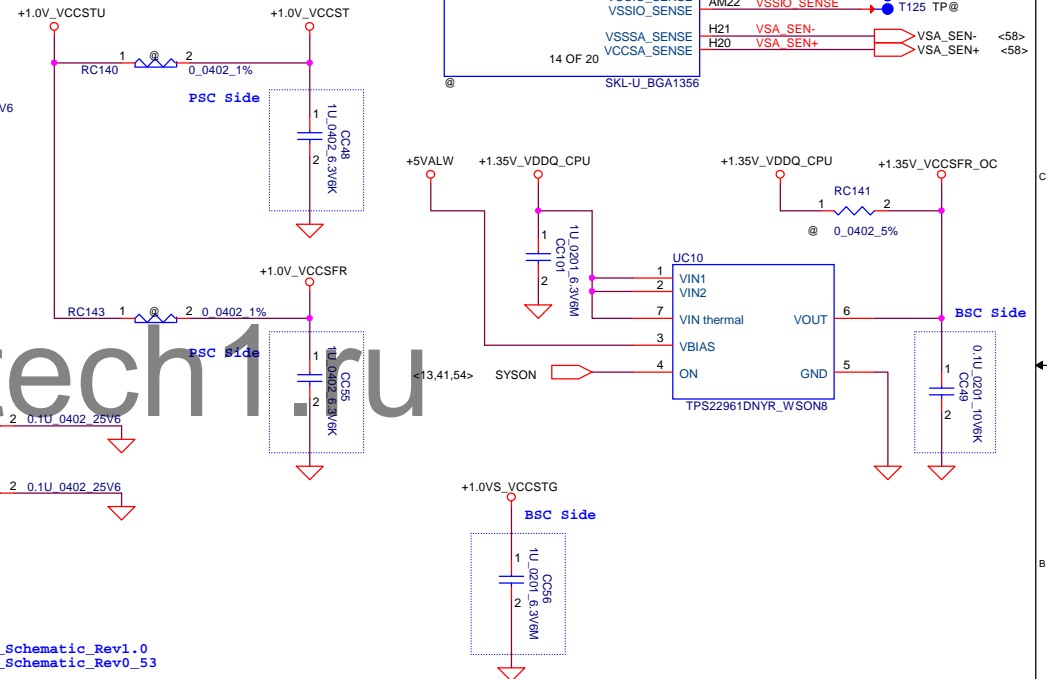
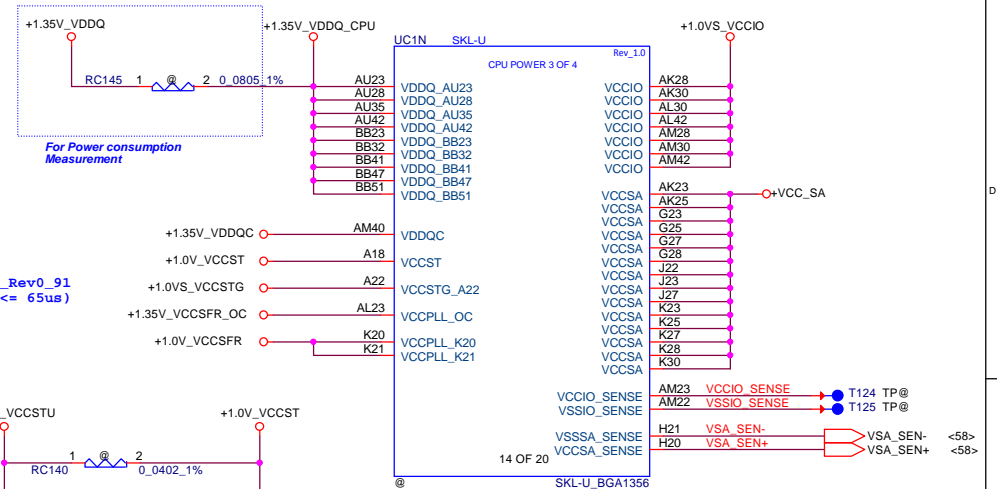
+1.0V_PRIM TO +1.0VS_VCCSTG / +1.0VS_VCCIO



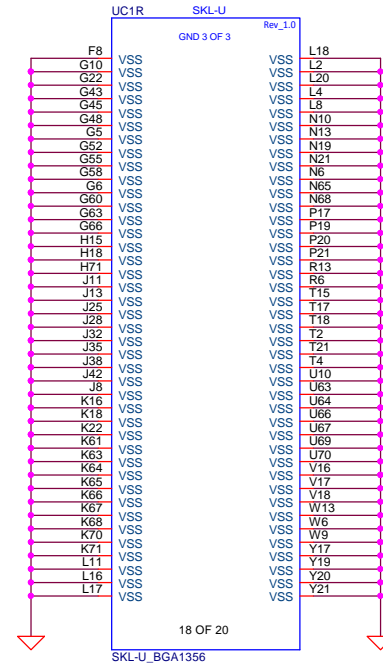
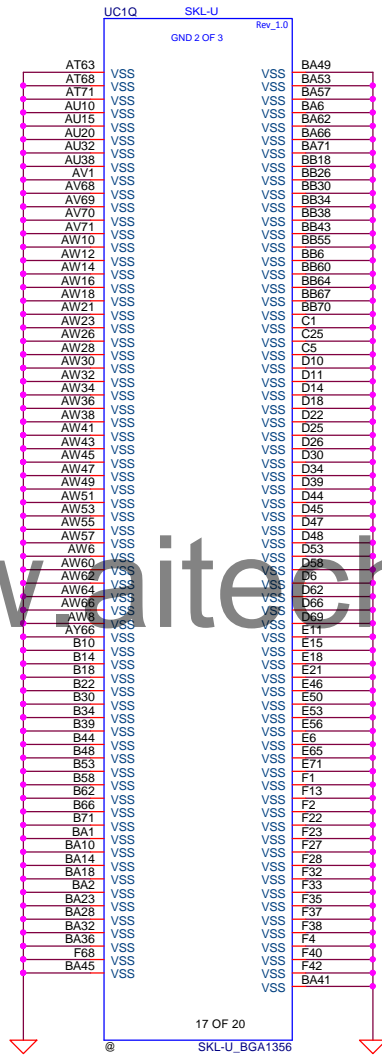
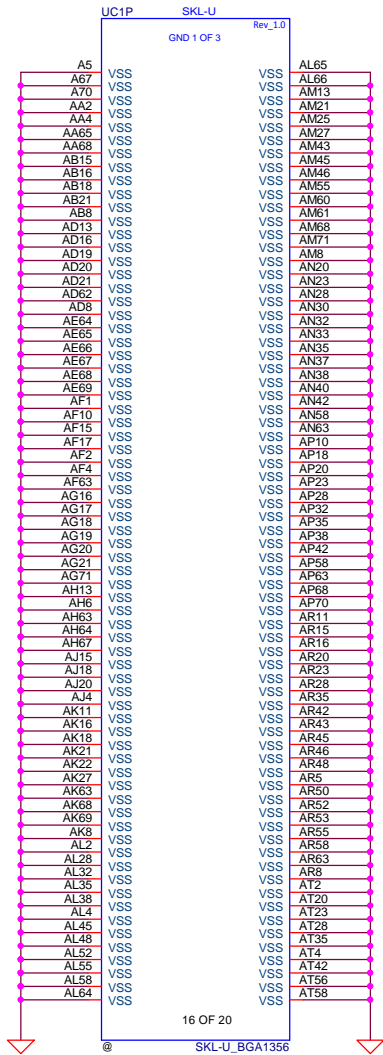
RC208 Follow 544669_SKL_U_DDR3L_RVP7_Schematic_Rev1.0
RC208 Follow 544669_SKL_U_DDR3L_RVP7_Schematic_Rev0_53



CC93 Follow 543016_SKL UY PDG_rev1_3

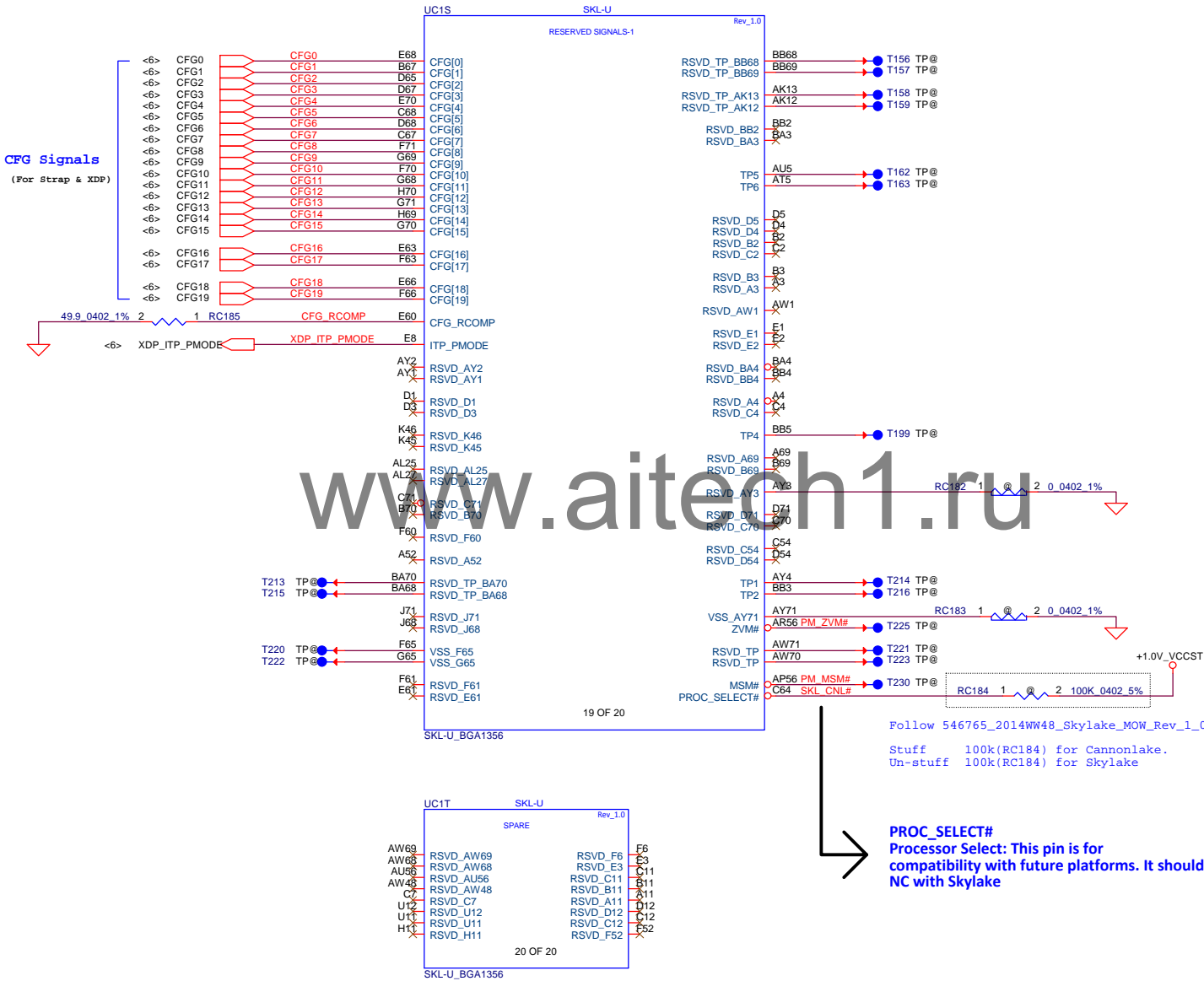


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				Size	Document Number	Rev
				LA-C901P		
				Date:	Tuesday, August 04, 2015	Sheet 13 of 63



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Issued Date	2015/01/06	Deciphered Date	2016/01/06	Title	SKL-U(11/12)GND
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Display Port Presence Strap	
CFG4	<p>1 : Disabled; No Physical Display Port attached to Embedded Display Port</p> <p>0 : Enabled; An external Display Port device is connected to the Embedded Display Port</p>



For 2+3e Solution

PM_ZVM#
Zero Voltage Mode: Control Signal to OPC VR, when low OPC VR output is 0V.

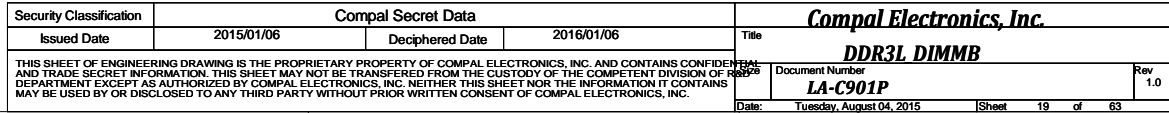
PM_MSM#
Minimum Speed Mode: Control signal to VccEOPIO VR (connected only in 2 VR solution for OPC).

Follow 546765_2014WW48_Skylake_MOW_Rev_1_0

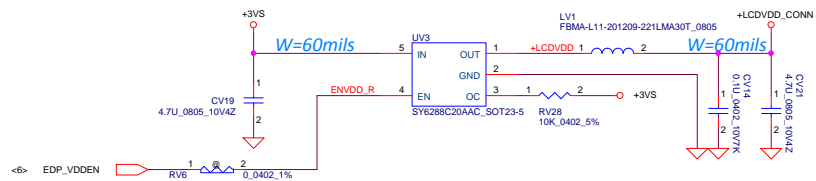
Stuff 100k(RC184) for Cannonlake.

Un-stuff 100k(RC184) for Skylake

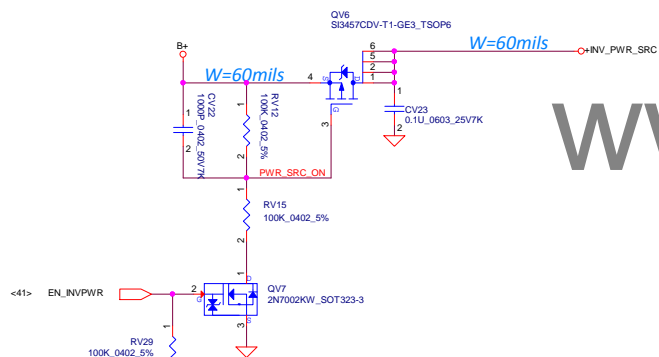
PROC_SELECT#
Processor Select: This pin is for compatibility with future platforms. It should NC with Skylake



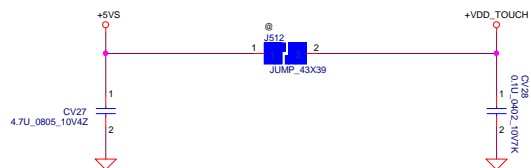
LCD power control



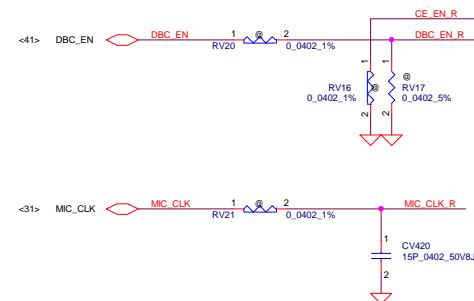
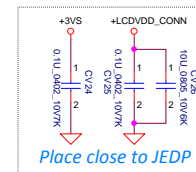
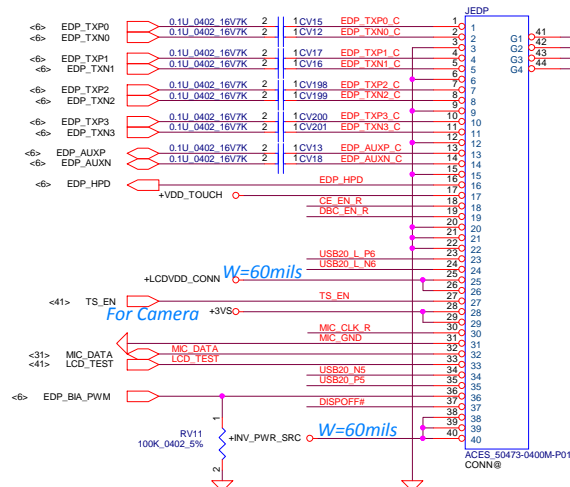
LCD backlight power control



Touch screen panel power control



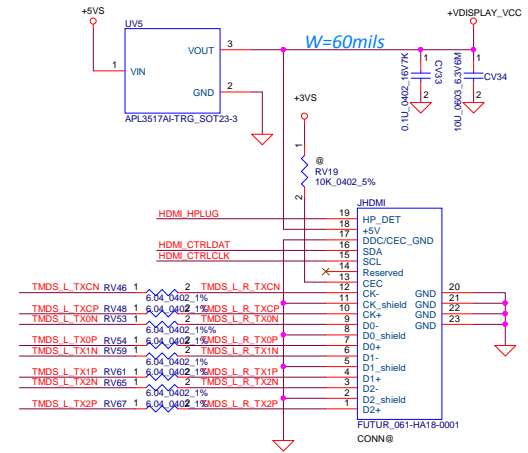
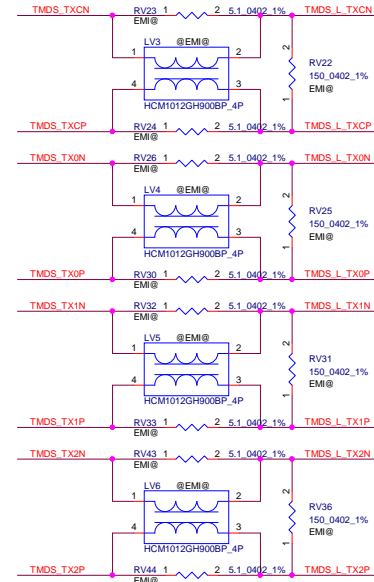
eDP connector



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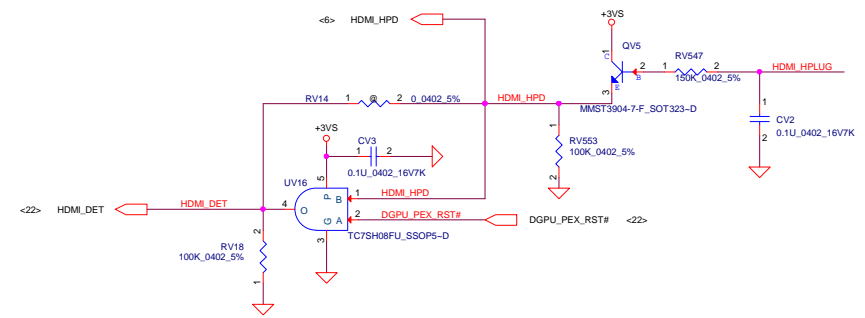
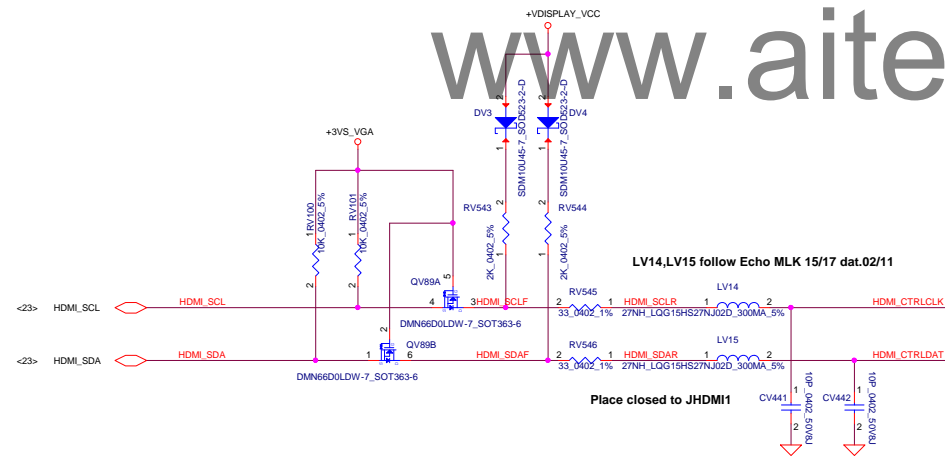
Security Classification		Compal Secret Data		Title	
Issued Date		Deciphered Date		eDP/webcam/touch	
2015/01/06		2016/01/06		LA-C901P	
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Date		Tuesdays, August 04, 2015		Sheet 20 of 63	

Place close to JHDMI

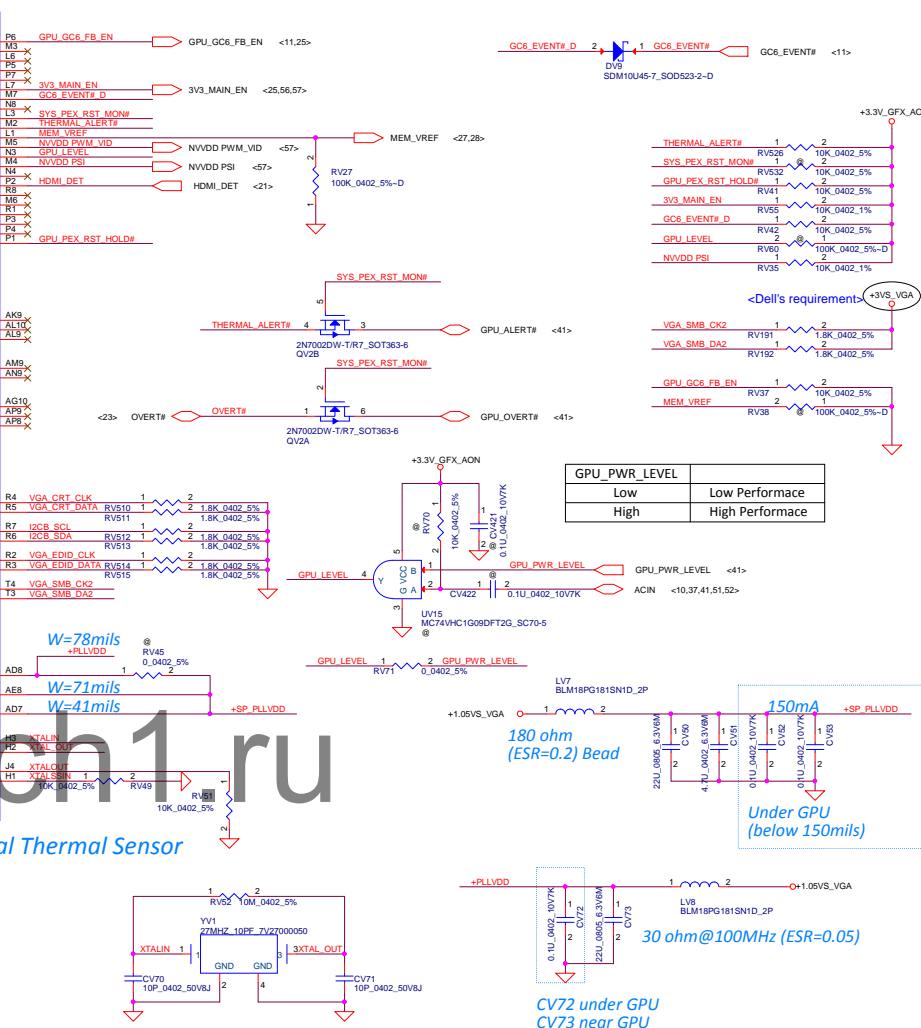
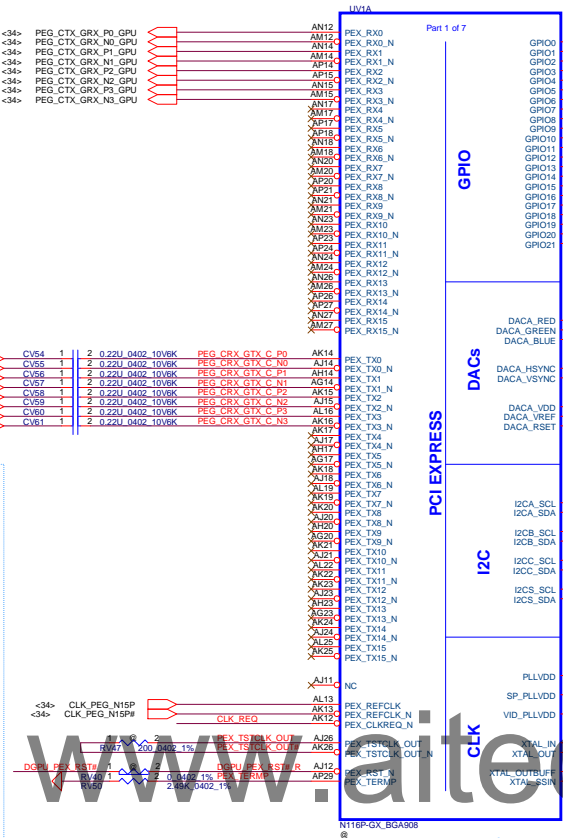
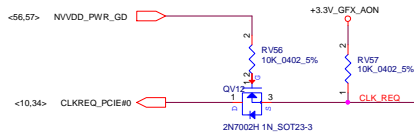
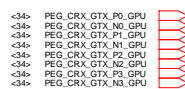


ROYALTY HDMI W/LOGO
CPN:RO000002HM

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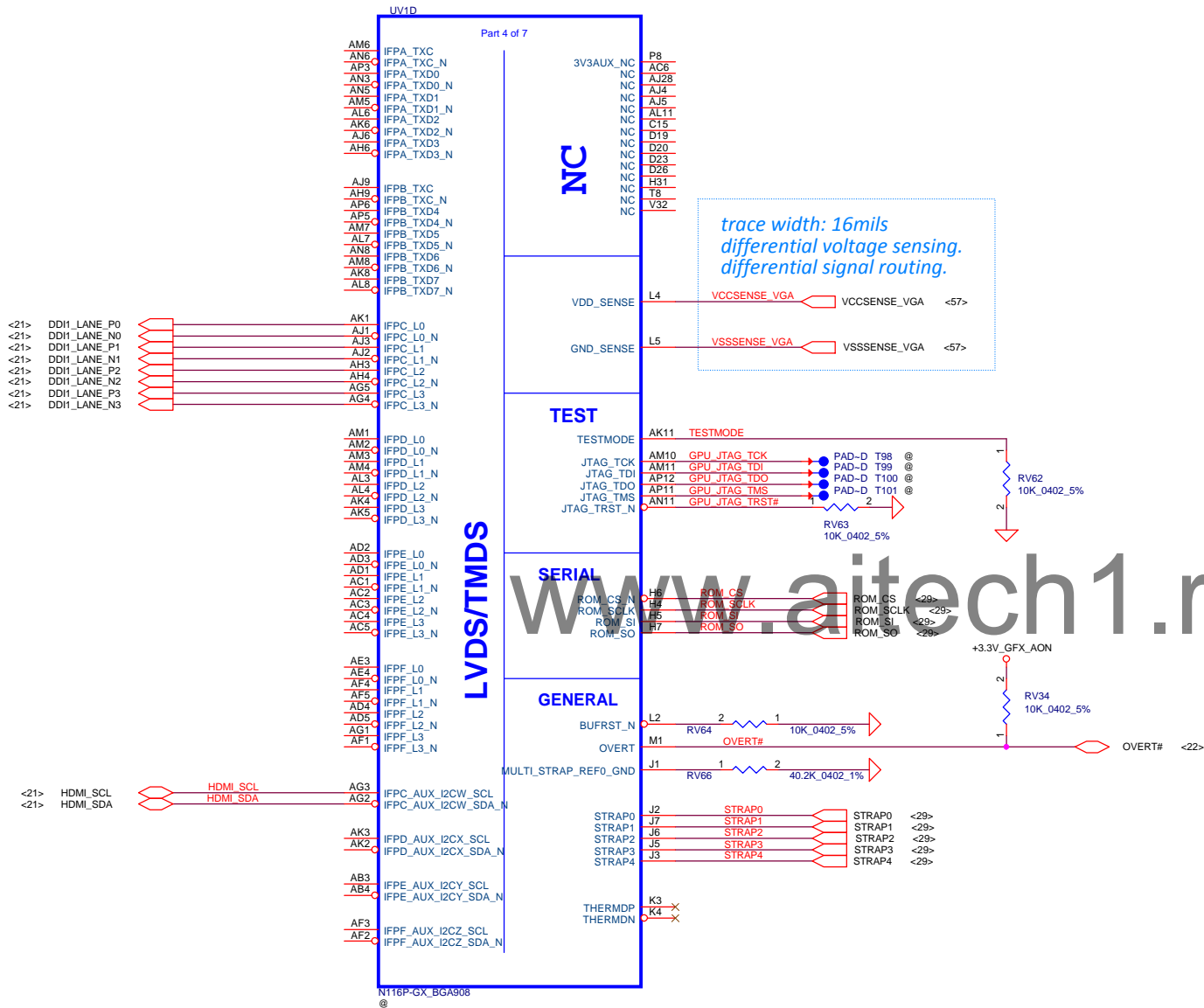


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2015/01/06		2016/01/06		Document Number	
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GPU_PWR_LEVEL	
Low	Low Performace
High	High Performace

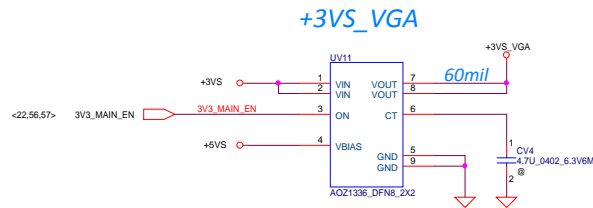
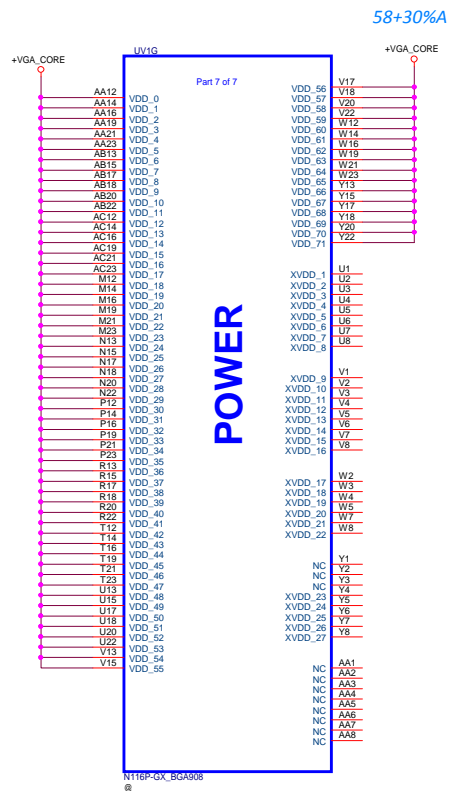
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Issued Date	2015/01/06	Deciphered Date	2016/01/06	Part Number		Rev
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				Document Number		
				LA-C901P		
Date:	Tuesday, August 4, 2015		Sheet	22	of	63



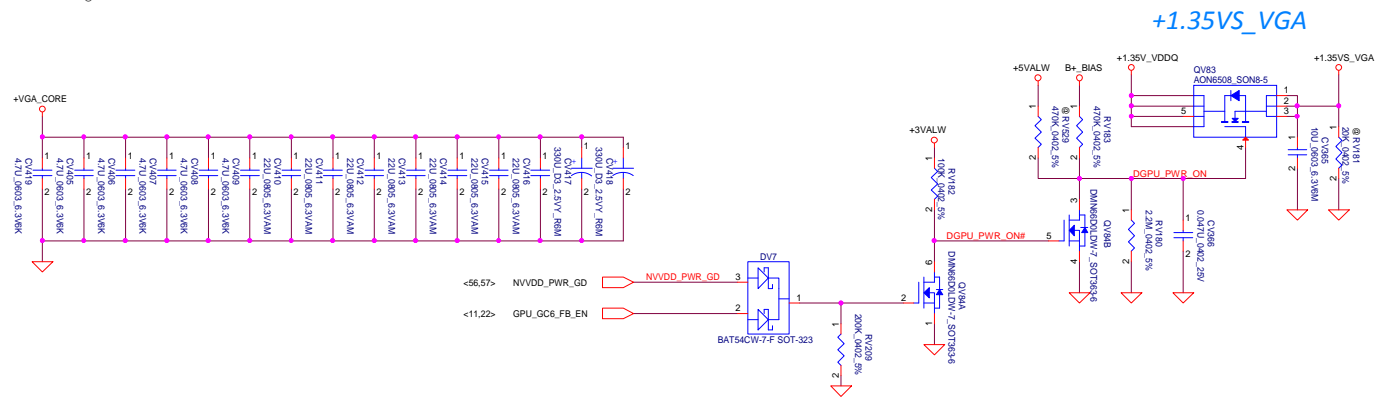
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2015/01/06		Deciphered Date		2016/01/06		Title	
										N16P HDMI	
										Document Number	
										LA-C901P	
										Date	
										Tuesday, August 04, 2015	
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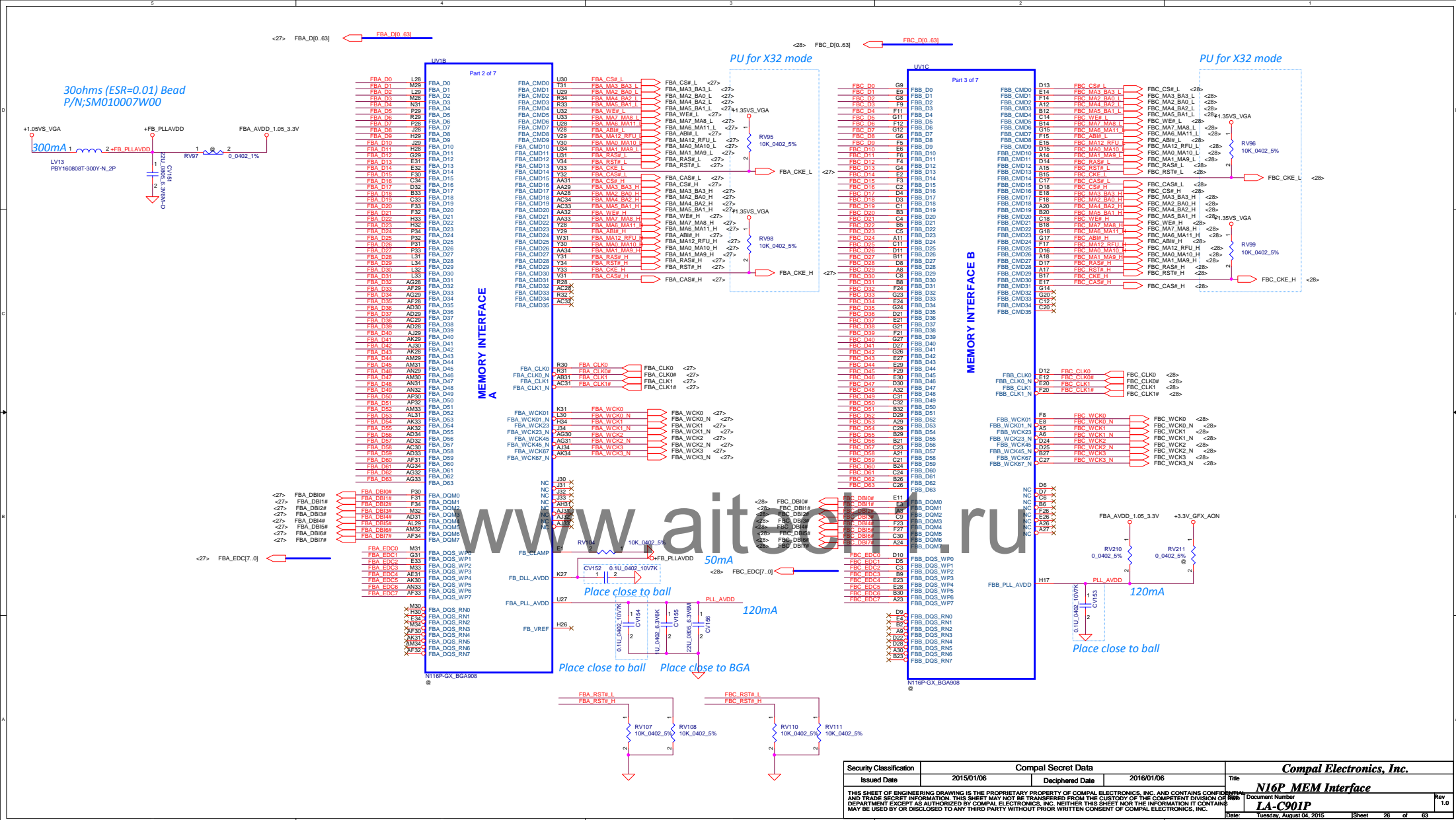
Size
Rev
1.0



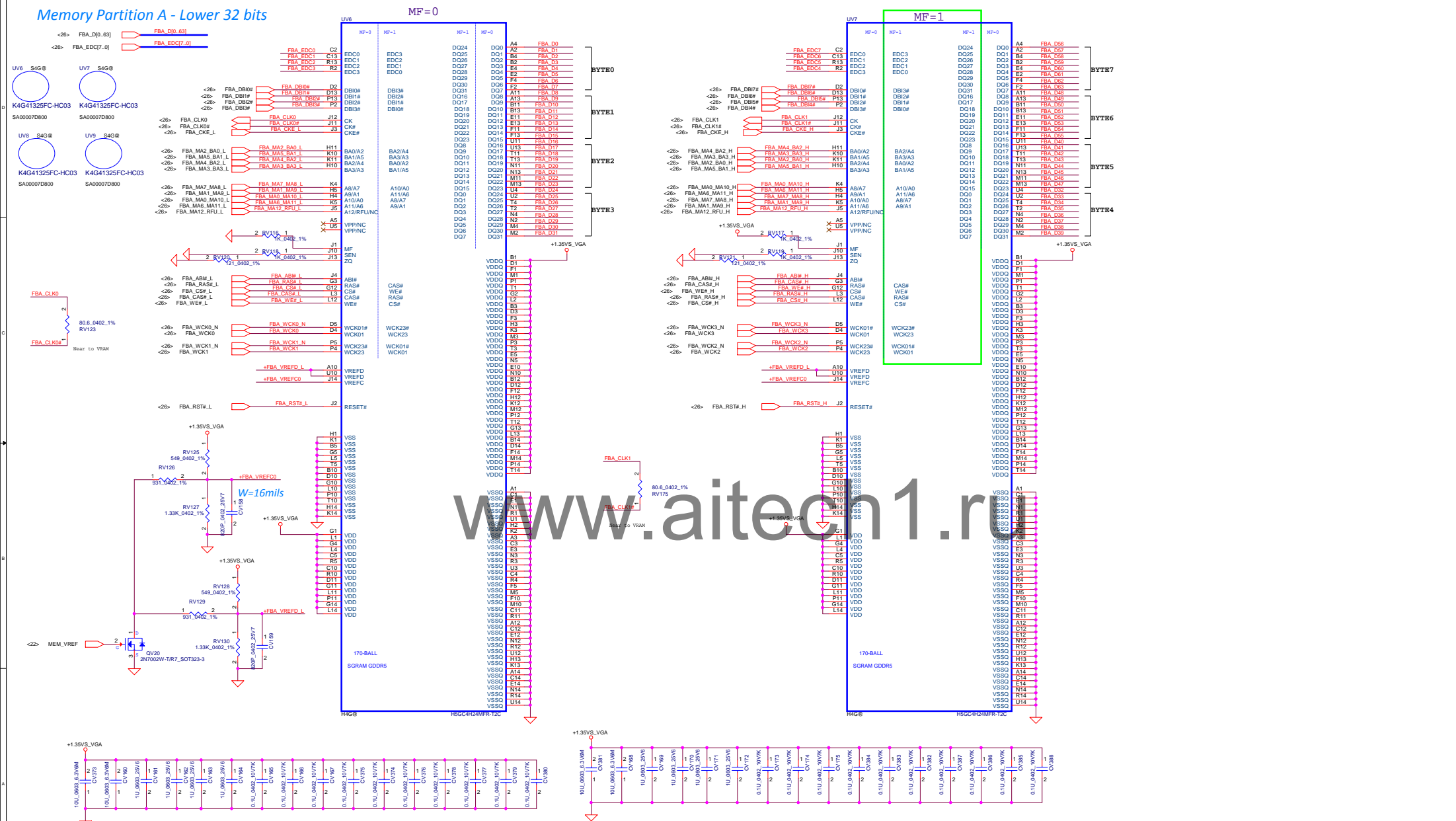
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				Document Number
				LA-C901P
				Date
				Tuesday, August 04, 2015
				Sheet
				25 of 63

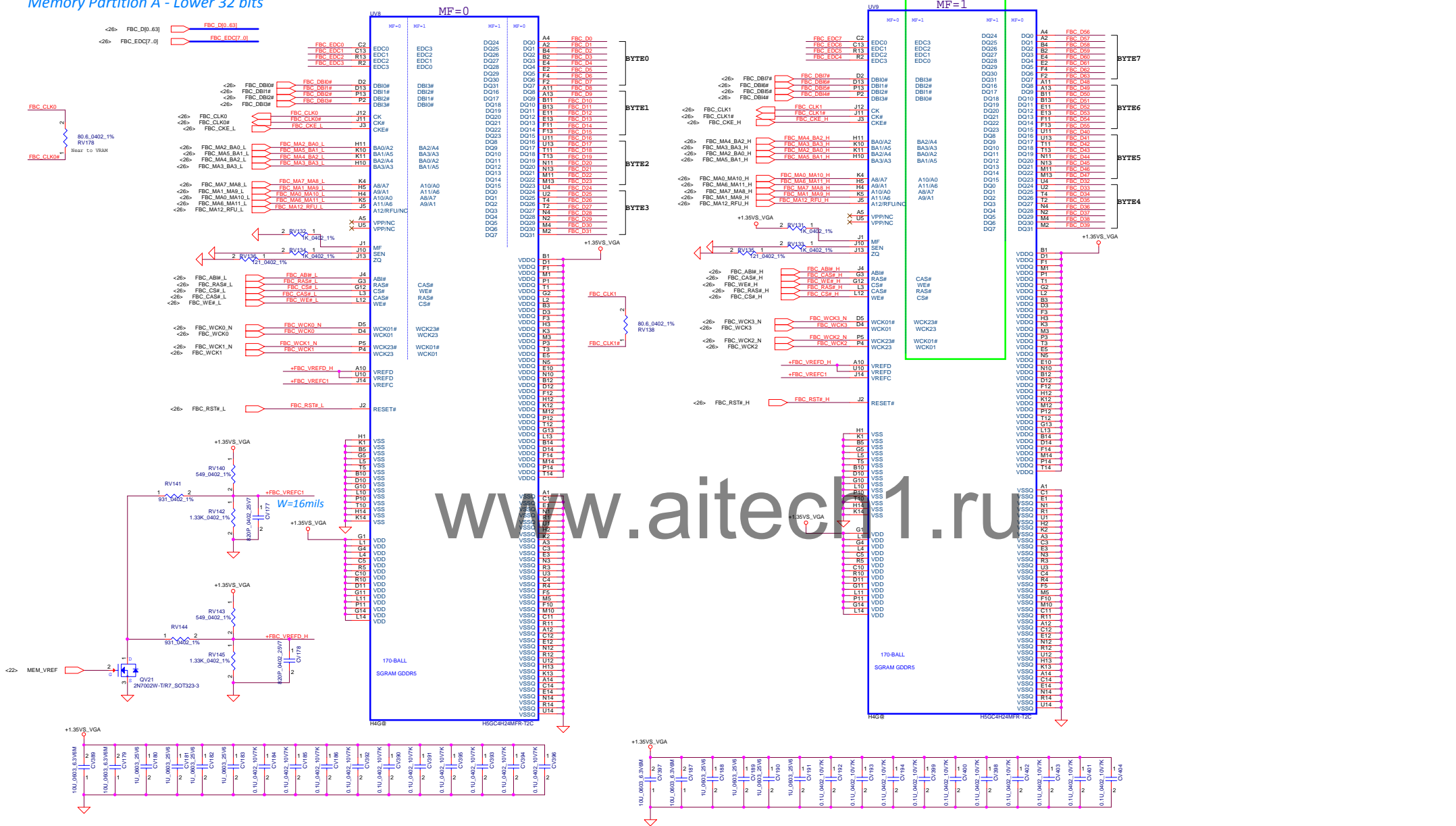


Memory Partition A - Lower 32 bits

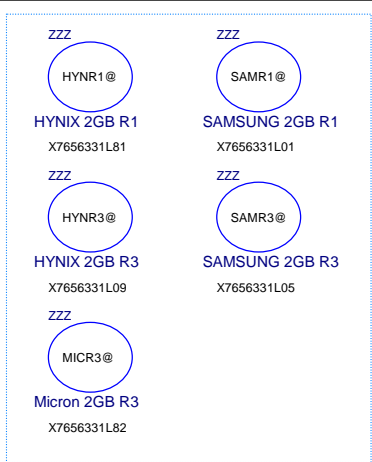


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Date:	January 04, 2015	Sheet	27	of	63

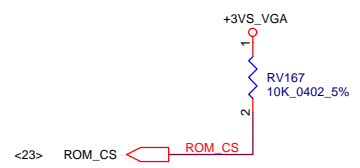
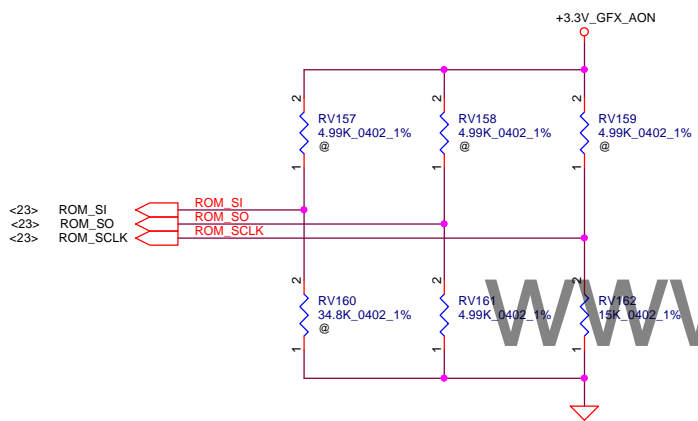
Memory Partition A - Lower 32 bits



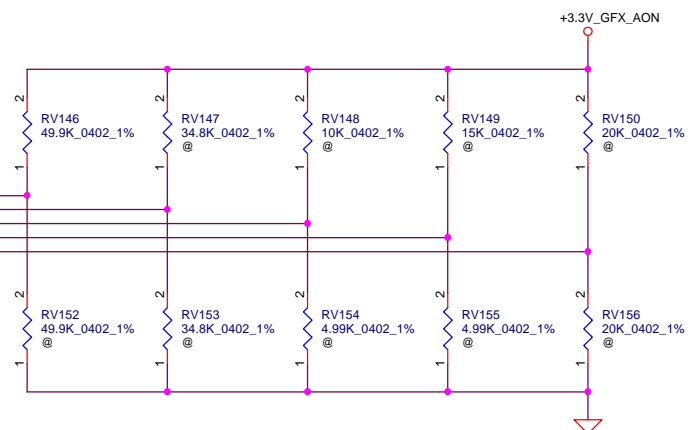
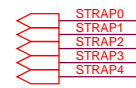
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			Date: Tuesday, April 04, 2015 Sheet: 28 of 63	



X7656331L01 : SAMR1@
X7656331L81 : HYNR1@
X7656331L05 : SAMR3@
X7656331L09 : HYNR3@



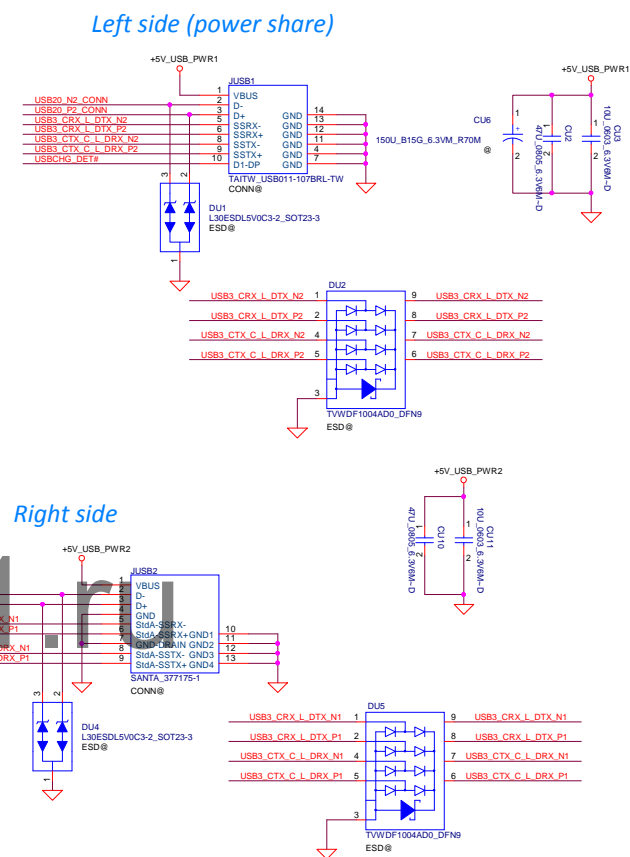
<23> STRAP0
<23> STRAP1
<23> STRAP2
<23> STRAP3
<23> STRAP4



SA00007D800 S IC D5 128M32 K4G41325FC-HC03 FBGA 170P
SA00007UZ1L S IC D5 128M32 EDW4032BABG-60-F-R A31!
SA00008HQ0L S IC D5 128M32/3G H5GC4H24AJR-ROC FBGA
SA00008HQ1L S IC D5 128M32/3G H5GC4H24AJR-ROC A31!

GPU	FB Memory	GDDR5	ROM_SO	ROM_SCLK	ROM_SI	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N16P-GX	Samsung 2500MHZ	K4G41325FC-HC03	PD 4.99K	PD 4.99K	PD 20K	PU 49.9K	NA	NA	NA	NA
		256Mx16								
	Hynix 2500MHZ	H5GC4H24AJR-R0C	PD 4.99K	PD 4.99K	PD 34.8K	PU 49.9K	NA	NA	NA	NA
		256Mx16								

W25X20CL 2M-Bit/256K-byte



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From CPU RX

To N16P-GX TX

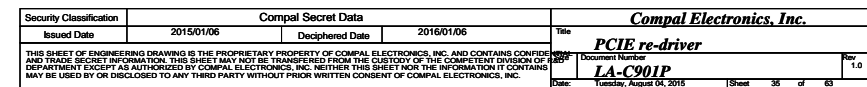
From CPU TX

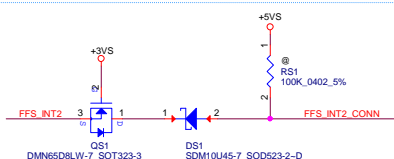
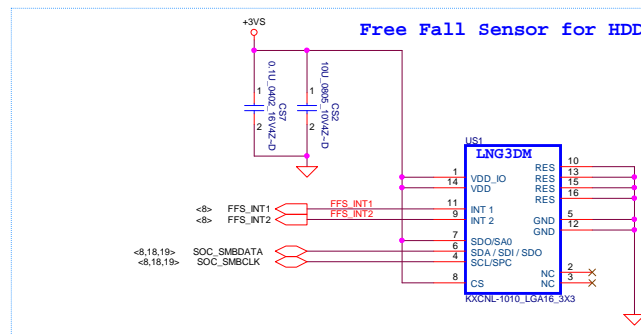
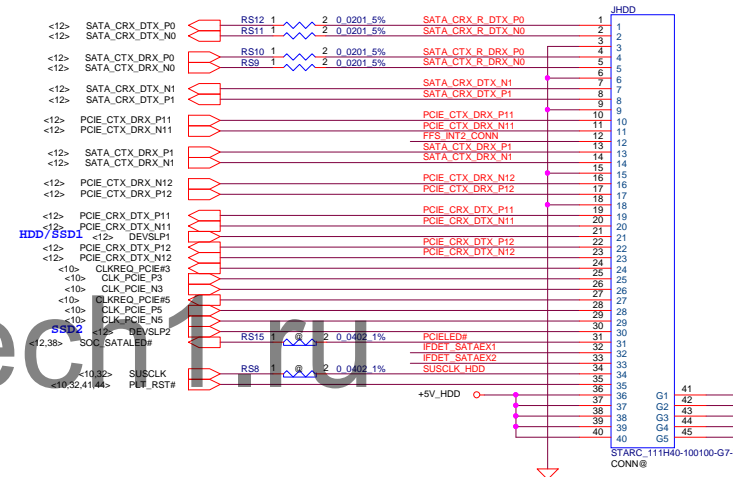
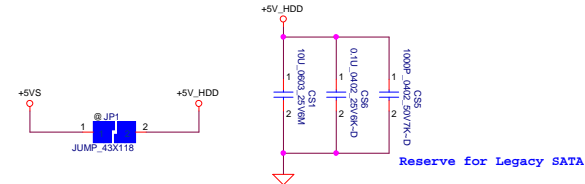
To N16P-GX RX

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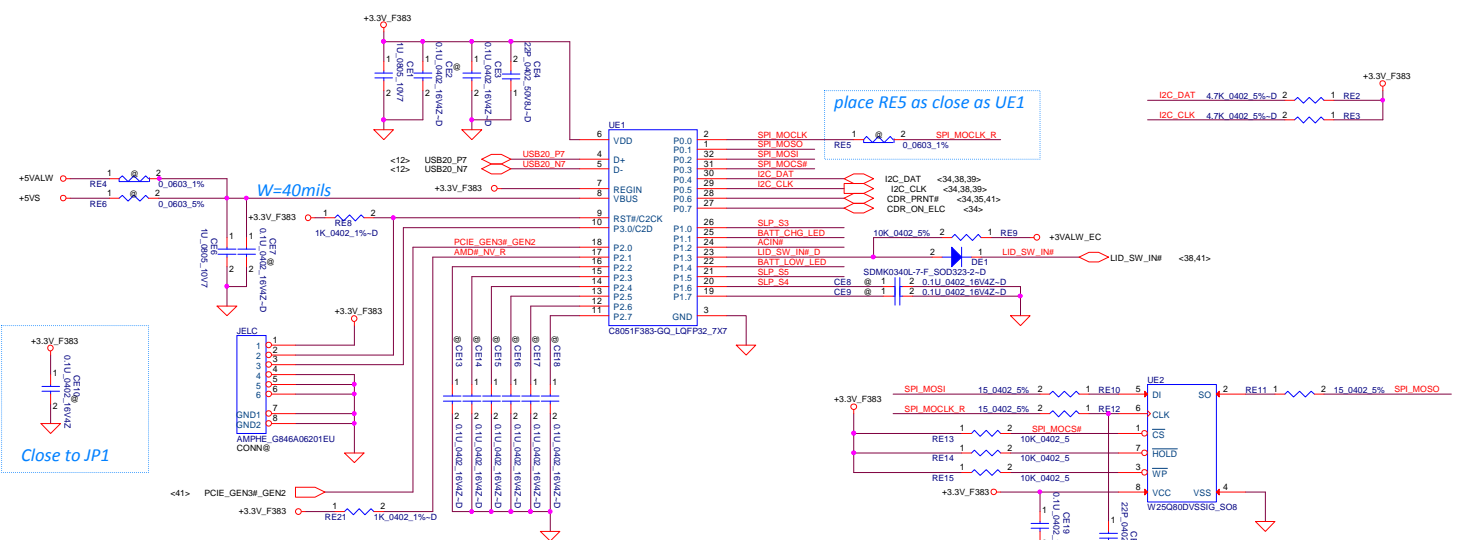
PCIE_CLK_BUFFER

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2015/01/06		2016/01/06		PCIE MUX/CLK BUFFER	
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Document Number				Rev	
LA-C901P				1.0	
Date		Version		Sheet	
January 03, 2015		1		34 of 63	

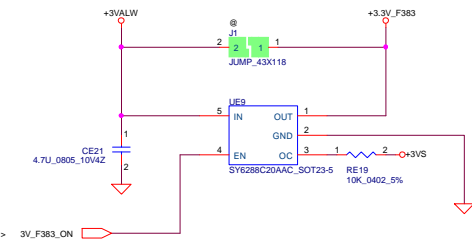
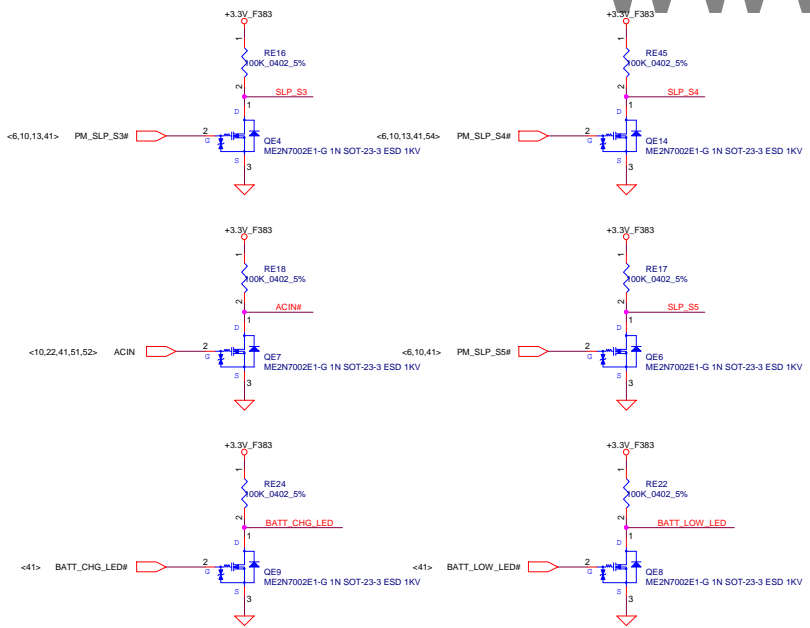




DET_SATA#/PCI-E	Module Type
0	SATA
1	PCI-E



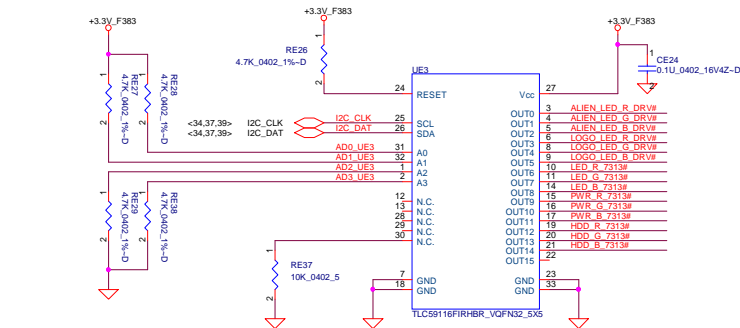
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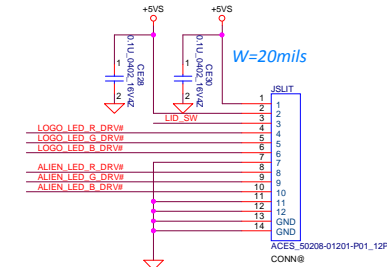
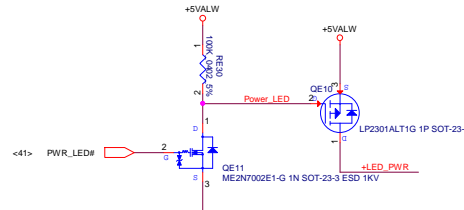
+3.3V_F383 behavior

	S0	S3	S4	S5
ACIN	ON	ON	ON	ON
BATT only	ON	ON	OFF	OFF

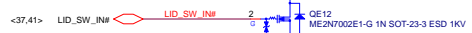
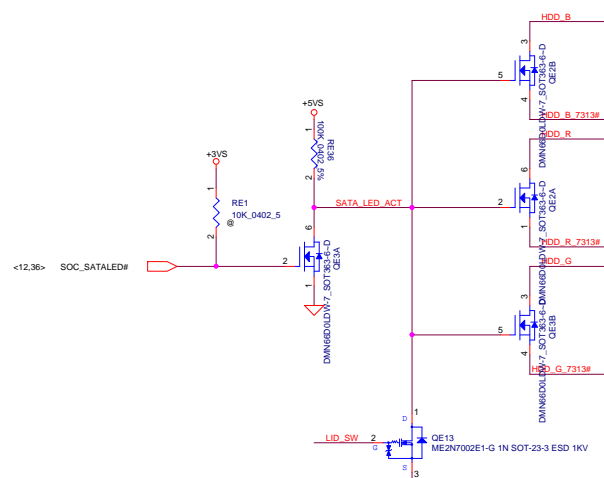
AC mode battery full in S5:turn off ELC controller



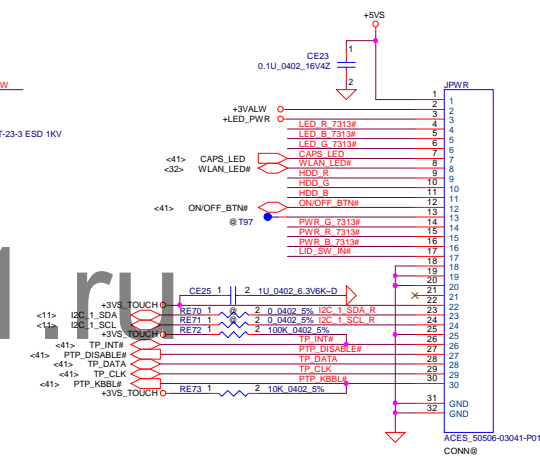
Power LED



Logic up LED board



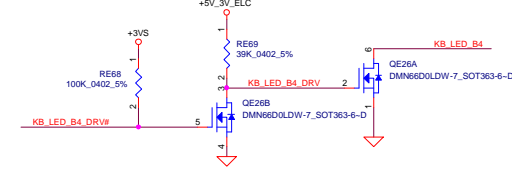
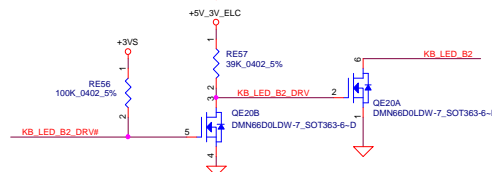
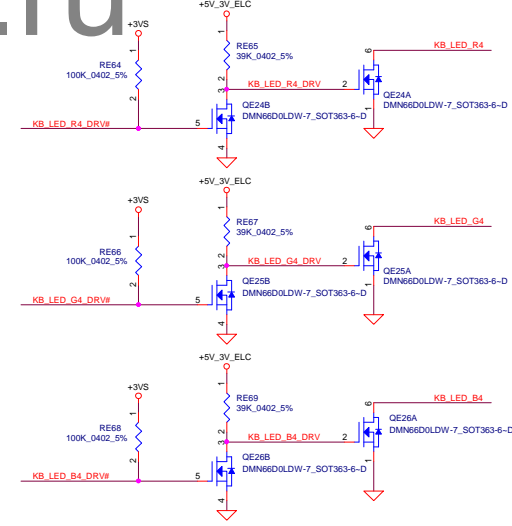
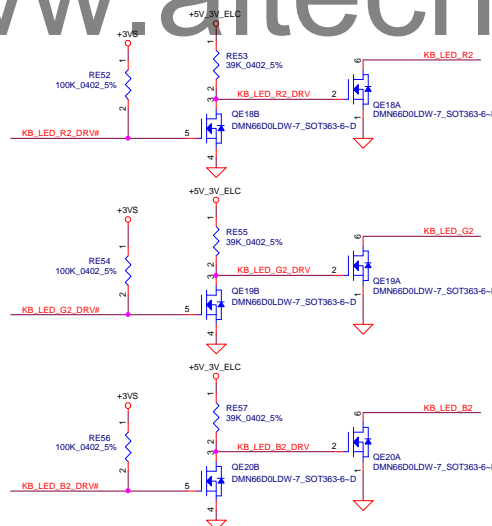
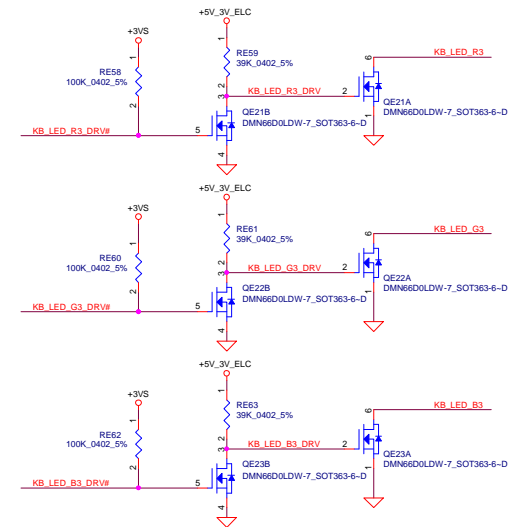
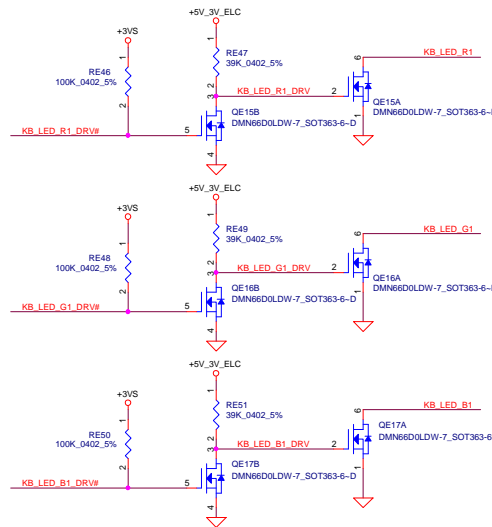
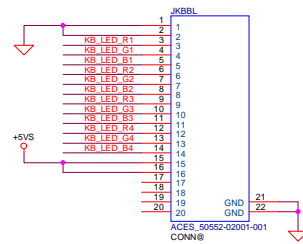
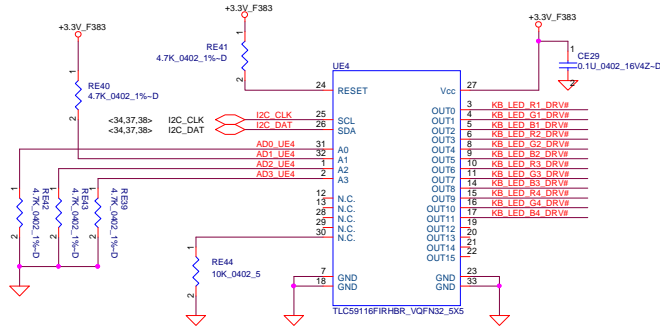
PTP pin define
VDD
I2C_DATA
I2C_CLK
GND
ATTN
PTP_DISABLE#(CLOSE LID)
PS2_DATA
PS2_CLK
PTP_KBBL#(KB BL)
NC



I2C address

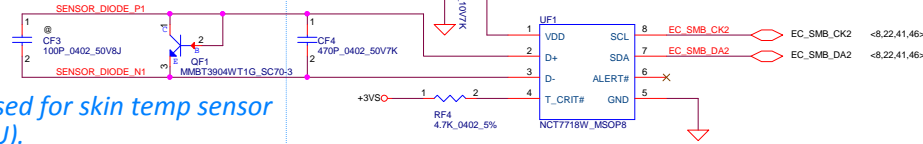
	A3	A2	A1	A0
UE1 (sheet 10 in Caldera board)	0	0	0	1
UE4 (sheet 39)	0	0	1	0
UE3 (sheet 38)	0	0	1	1
3rd LED drive (reserve)	0	1	0	0

Default use +3VS



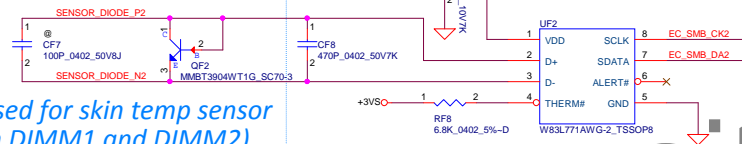
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Main:
NCT7718W(SA000067P00)
Address:1001_100xb(0x98)
Second:
ADM1032ARMZ-REEL(SA010320110)
Address:100_1100(0x4C)



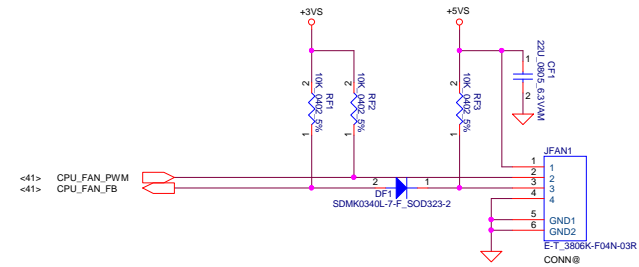
Diode circuit s used for skin temp sensor
(placed near CPU).
Place CF3 close to QF1 as possible.

Main:
W83L771AWG-2(SA00003PU00)
Address:1001_101xb(0x9A)
Second:
ADM1032ARMZ-2R(SA010320120)
Address:100_1101(0x4D)

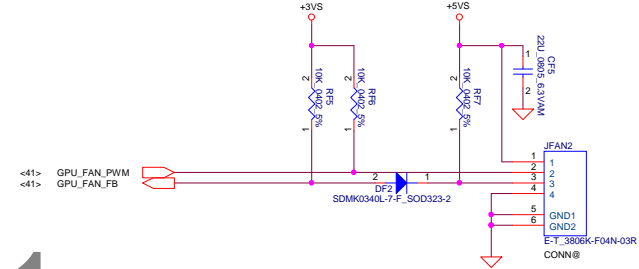


Diode circuit s used for skin temp sensor
(placed between DIMM1 and DIMM2).
Place CF7 close to QF2 as possible.

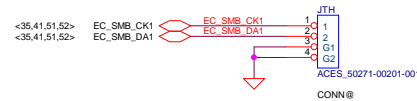
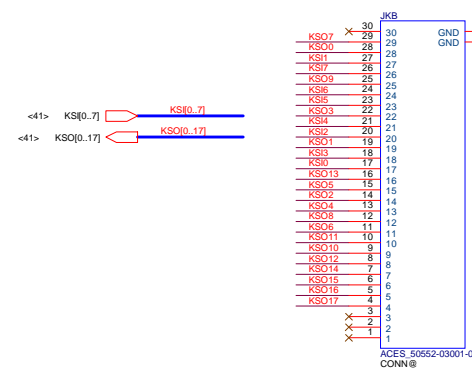
CPU FAN control circuit



GPU FAN control circuit

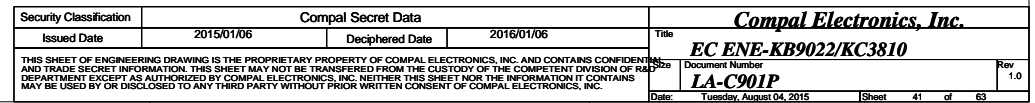


INT_KBD Connector

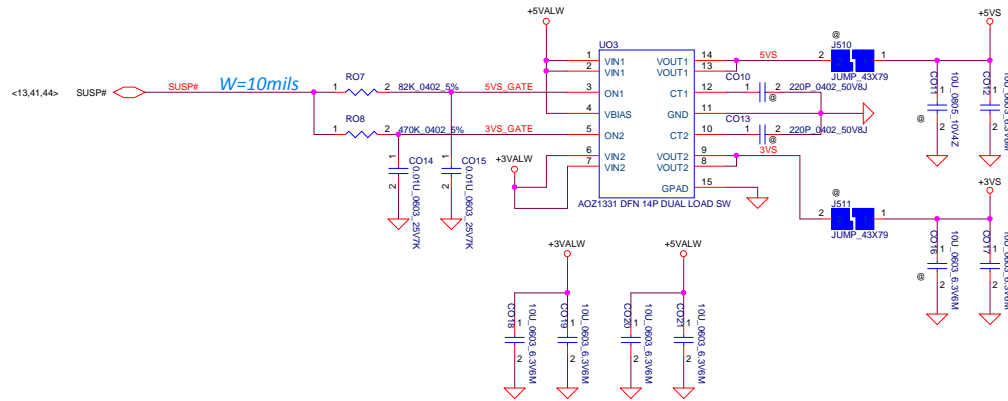


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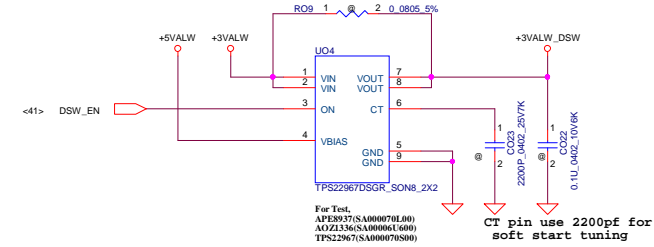
Security Classification	Compal Secret Data		Title	
Issued Date	2015/01/06	Deciphered Date	2016/01/06	Rev
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Date: Tuesday, August 04, 2015				Sheet 40 of 63



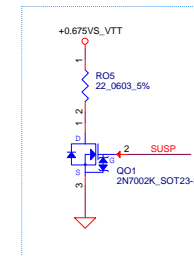
+5VS and +3VS switch



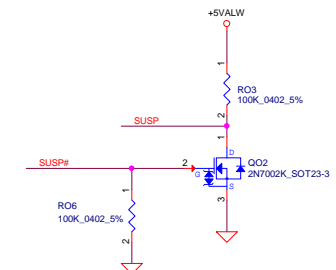
+3VALW TO +3VALW_DSW



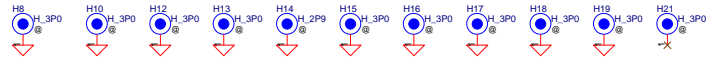
www.aitech1.ru



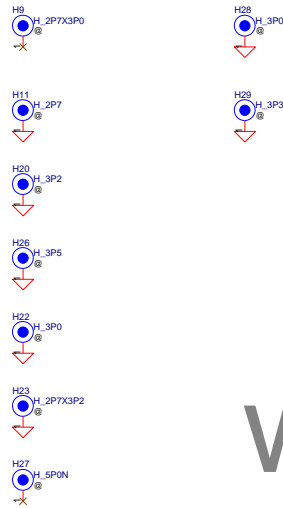
For Intel S3 power reduction



Screw Hole

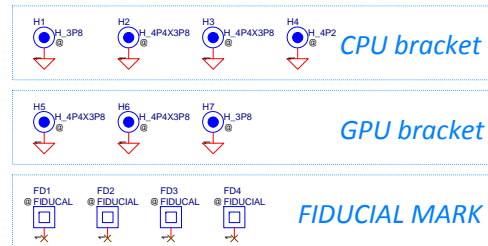


Echo MLK delete H24,H25

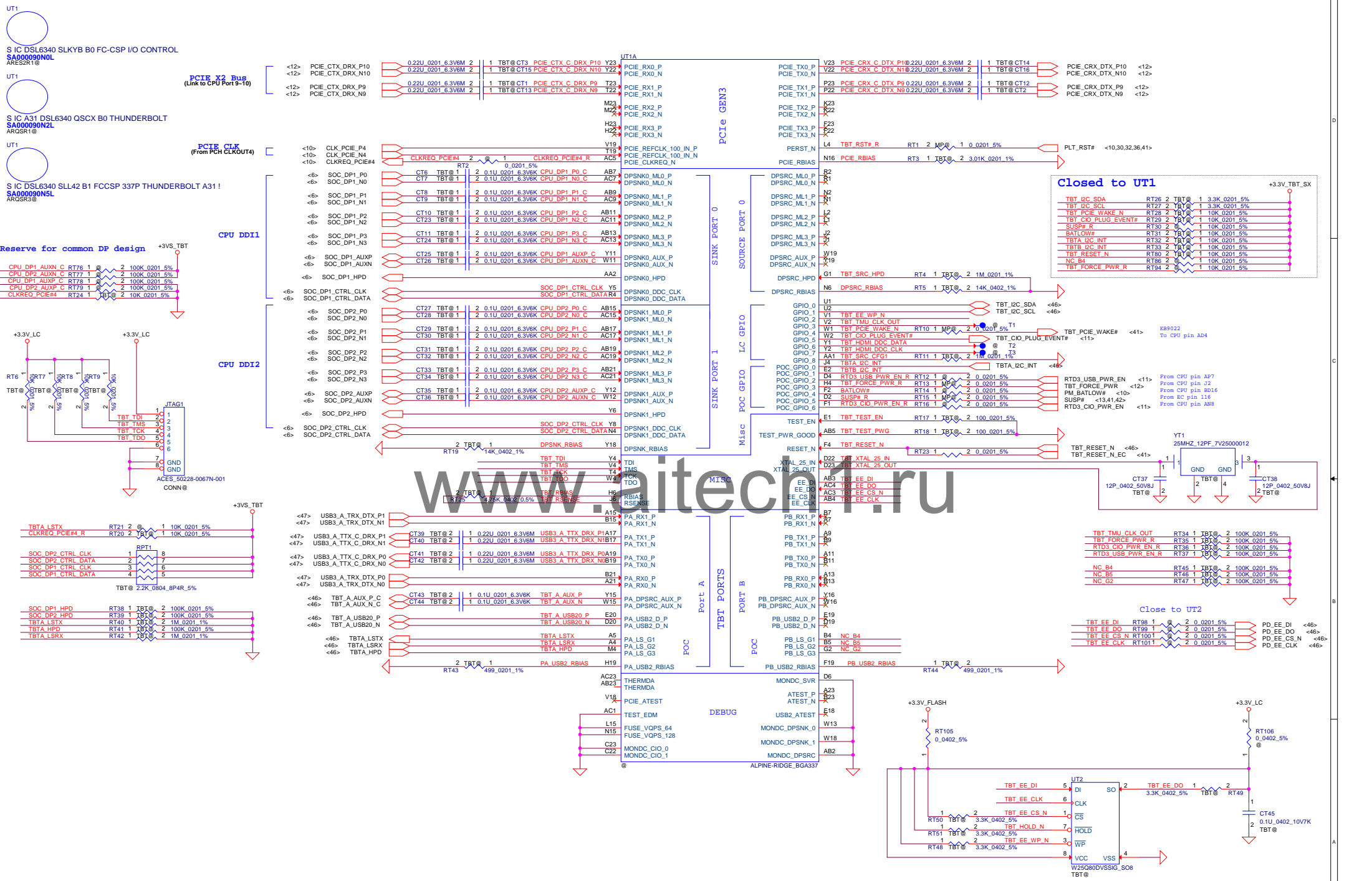


Add H28,H29 for USB3.1 type C

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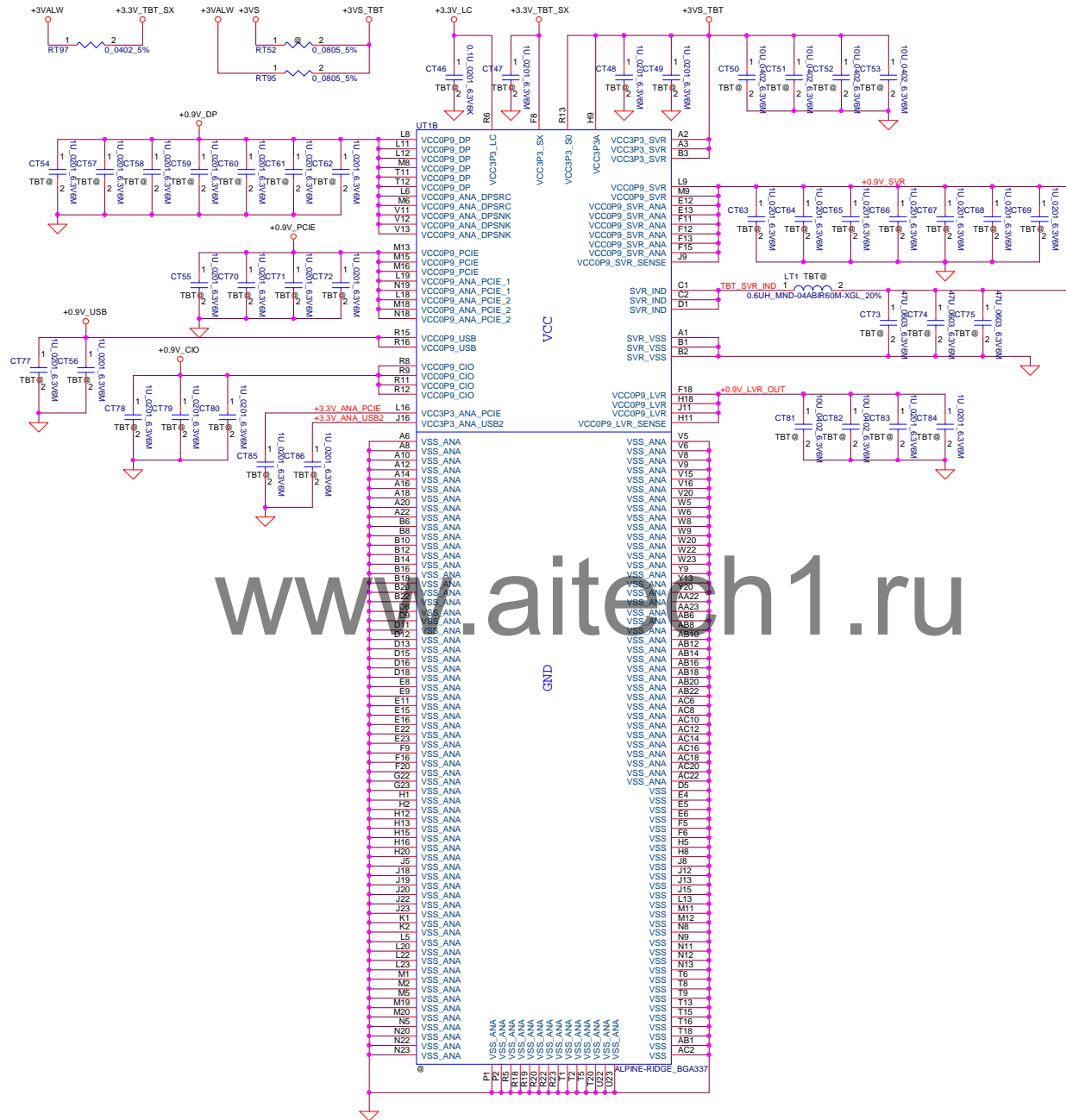


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				LA-C901P		1.0	
				Date:	Tuesday, August 04, 2015	Sheet	43 of 63

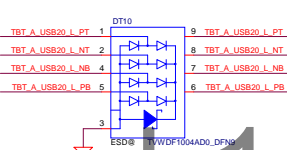
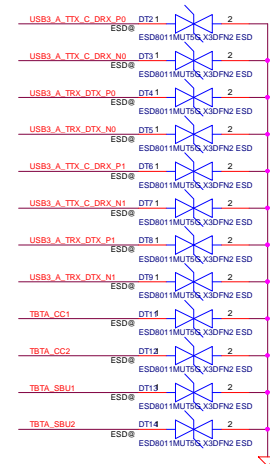
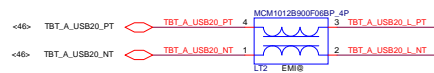
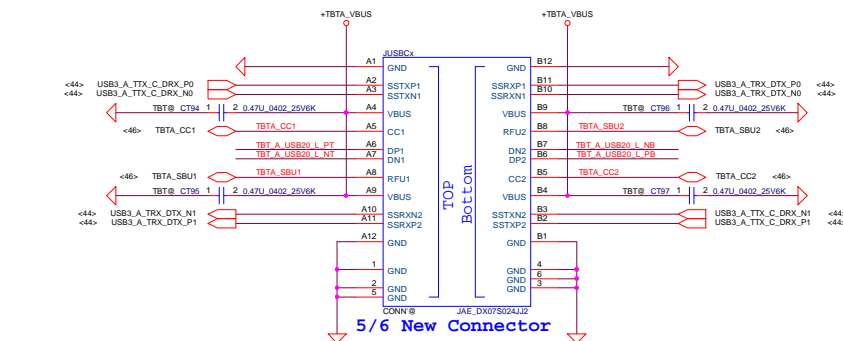


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Reserve RT104 follow E-team's design dat.04/07



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					Size	
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					1.0	



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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1				HW			
2				HW			
3				HW			
4				HW			
5				HW			
6				HW			
7				HW			
8				HW			
9				HW			
10				HW			
11				HW			
12				HW			
13				HW			
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42				HW			

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Compal Electronics, Inc.

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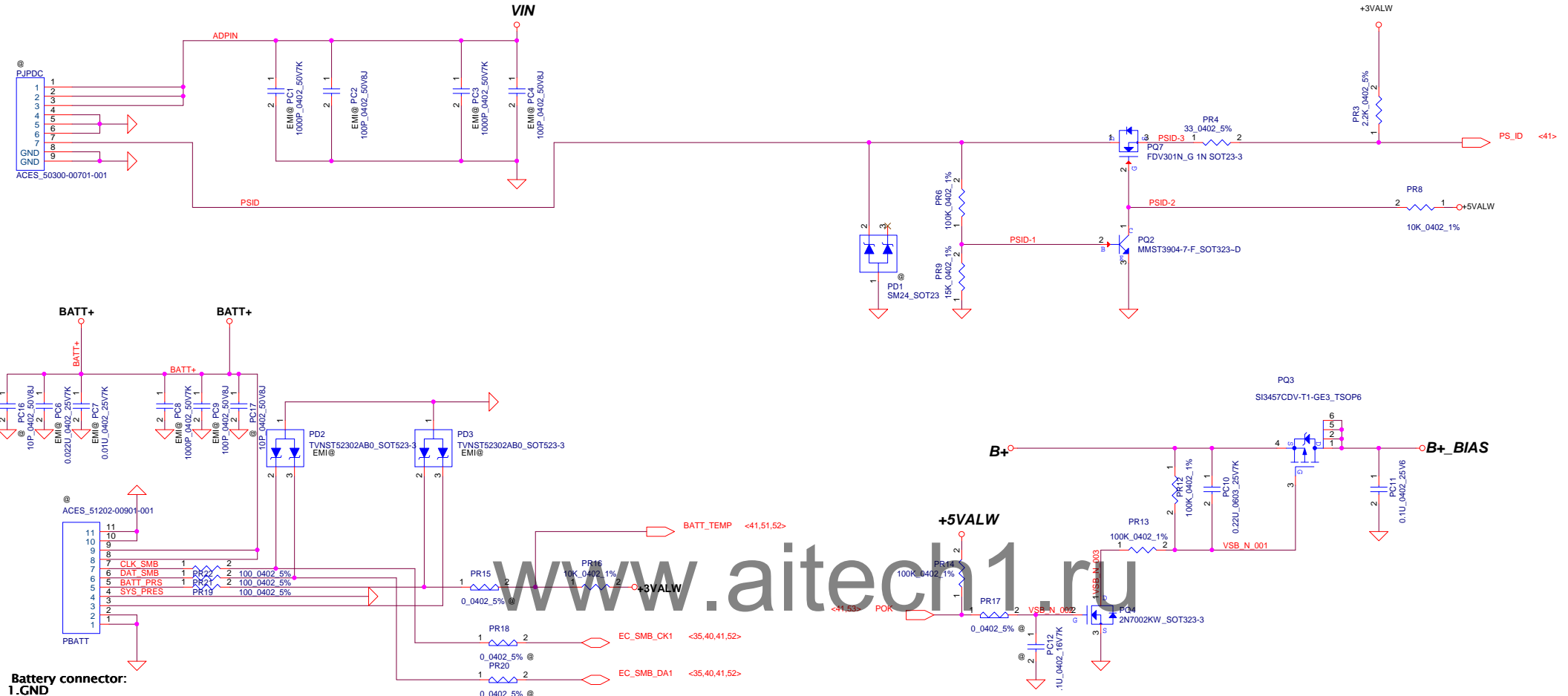
Rev 1.0

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
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48				HW			
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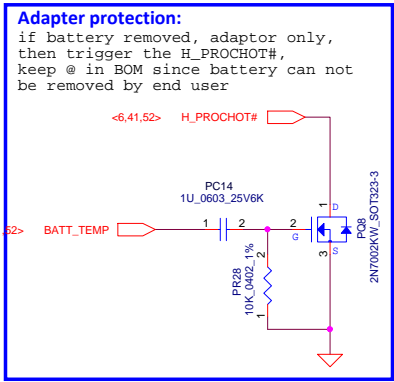
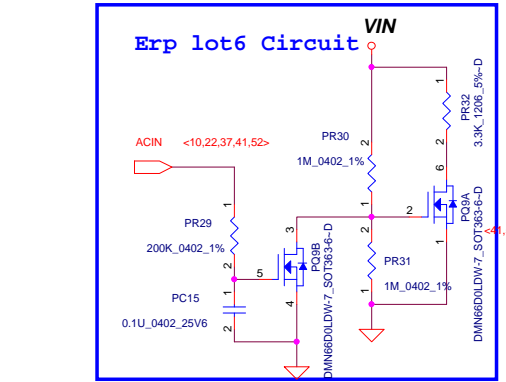
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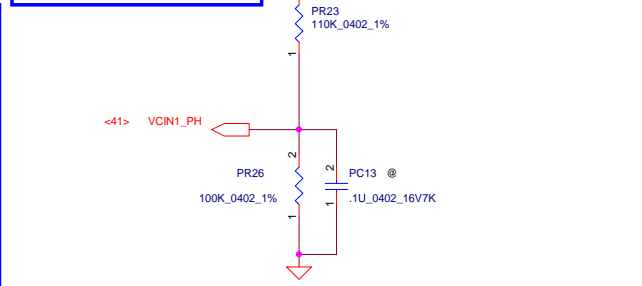
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Battery connector:
 1.GND
 2.GND
 3.BAT_ALERT
 4.SYS_PRES
 5.BATT_PRS
 6.DAT_SMB
 7.CLK_SMB
 8.BATT++
 9.BATT++
 10.GND
 11.GND

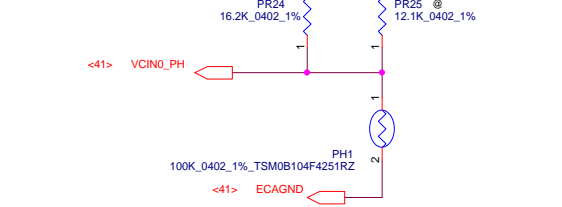


Adapter Protection
 VCIN1_PH setting
 Trigger point : 0.730V
 Recovery point : 0.635V



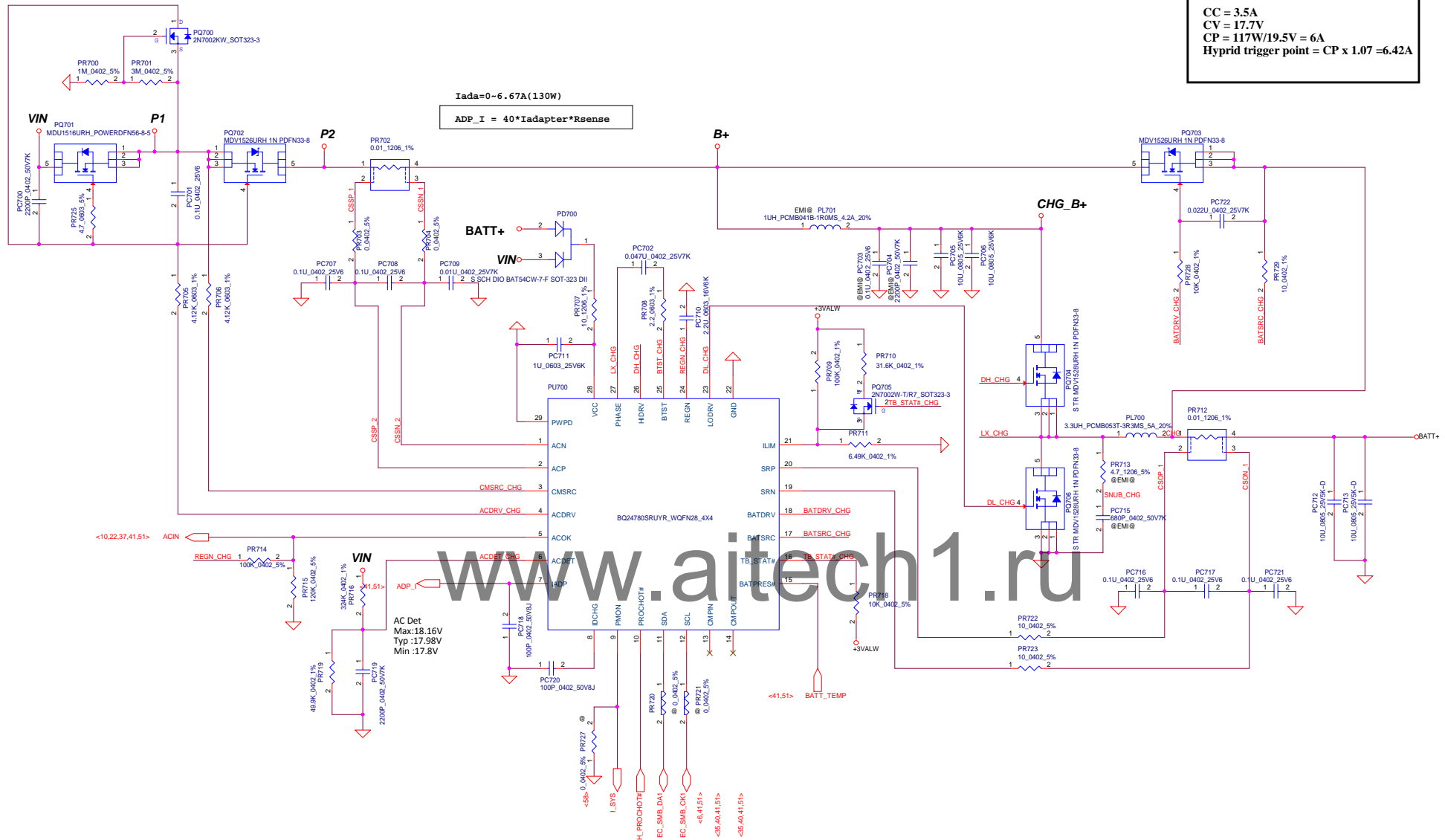
CPU thermal protection at 93 +/- 3 degree C

CPU OTP
 VCIN0_PH setting
 Trigger point : 1V
 Recovery point : 2.21V



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						Size		Document Number		Rev	
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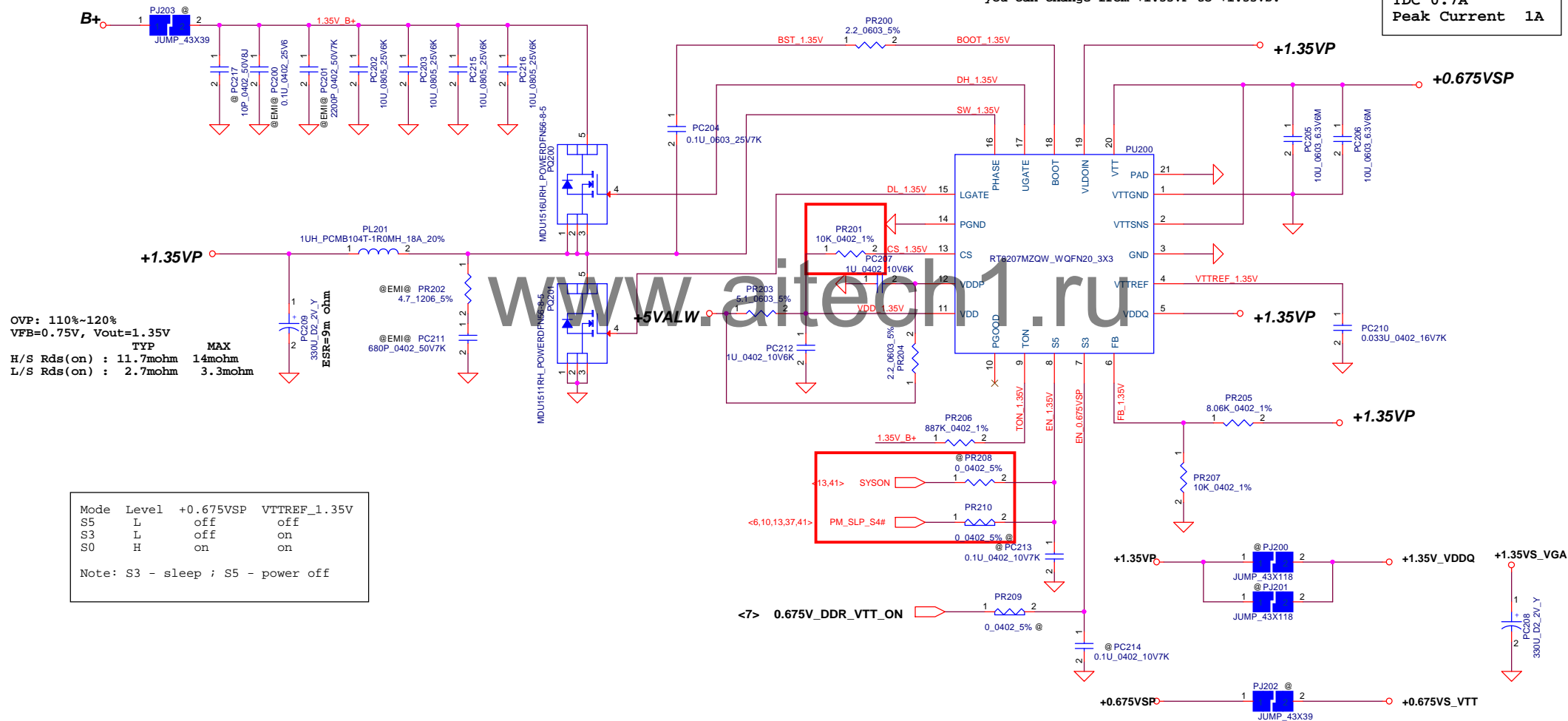
CC = 3.5A
CV = 17.7V
CP = 117W/19.5V = 6A
Hybrid trigger point = CP x 1.07 = 6.42A



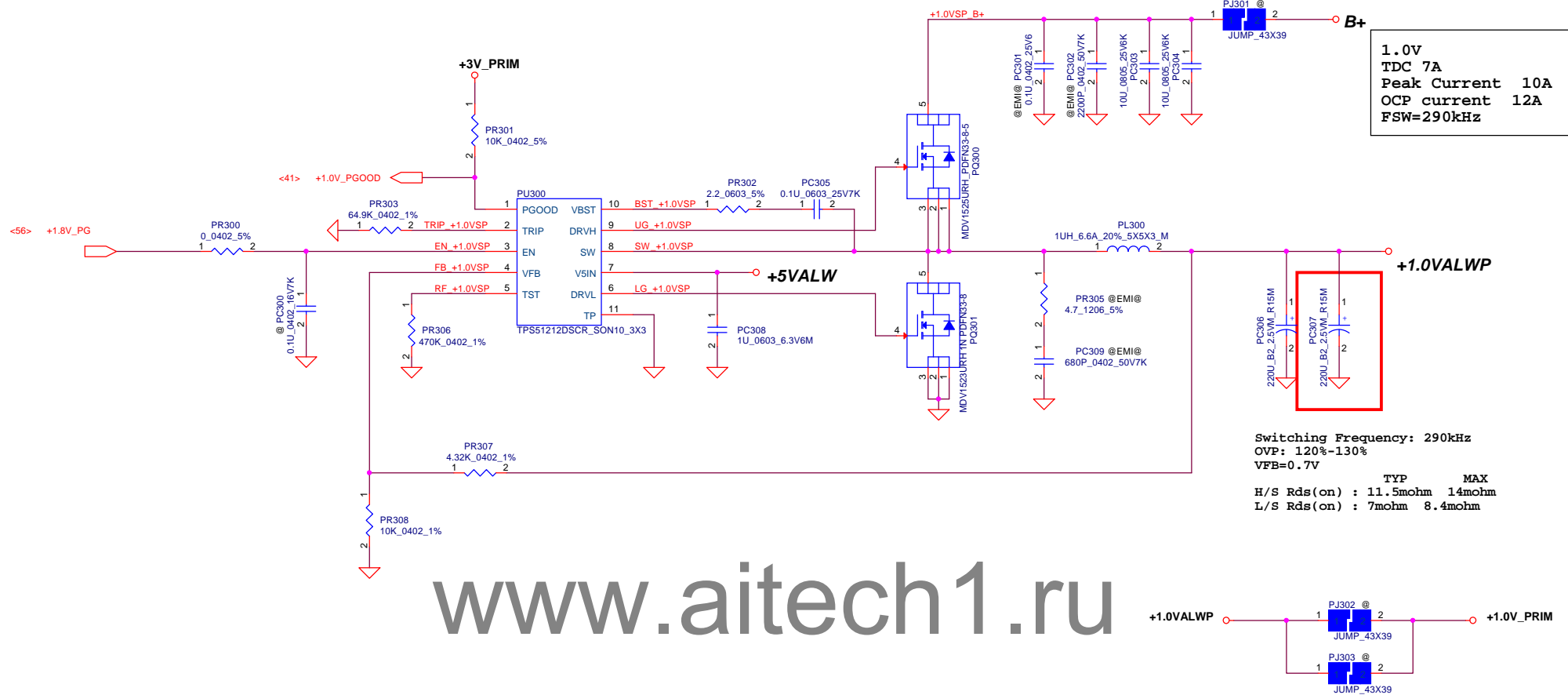
1.35VP
TDC=16.7A
Ipeak=24A
OCP=28.8A
Switching Frequency: 285kHz

Pin19 need pull separate from +1.35VP.
If you have +1.35V and +0.675V sequence question,
you can change from +1.35VP to +1.35VS.

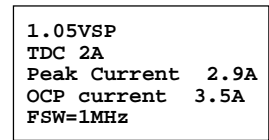
0.675Volt +/- 5%
TDC 0.7A
Peak Current 1A



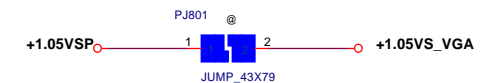
Security Classification		Compal Secret Data		Compal Electronics, Inc. PWR-1.35VP/0.675VSP	
Issued Date	2015/01/06	Deciphered Date	2016/01/06		
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$$V_{out} = 0.6V * (1 + R_{up}/R_{down})$$

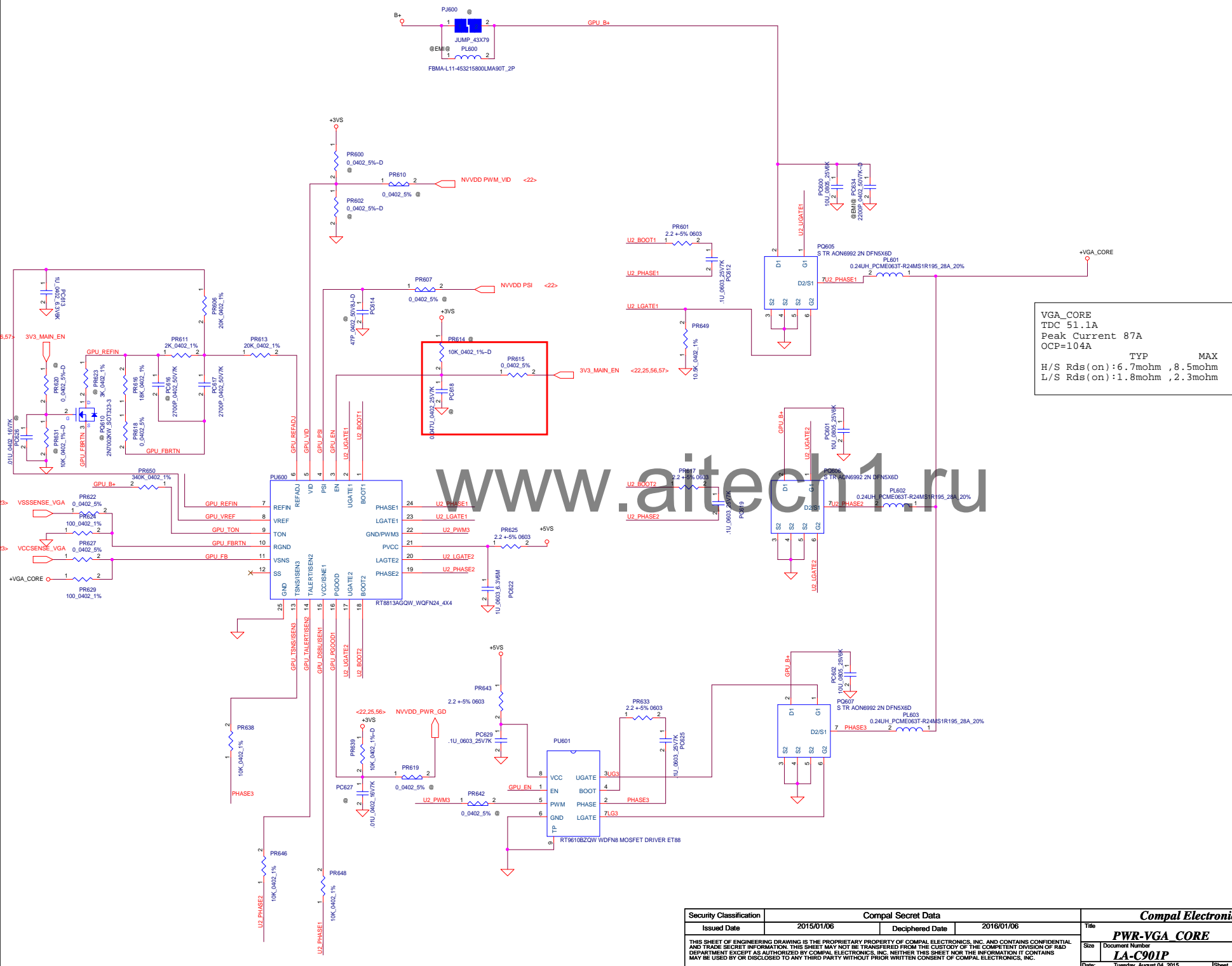
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```
+1.8V_PRIM
TDC 0.27A
```

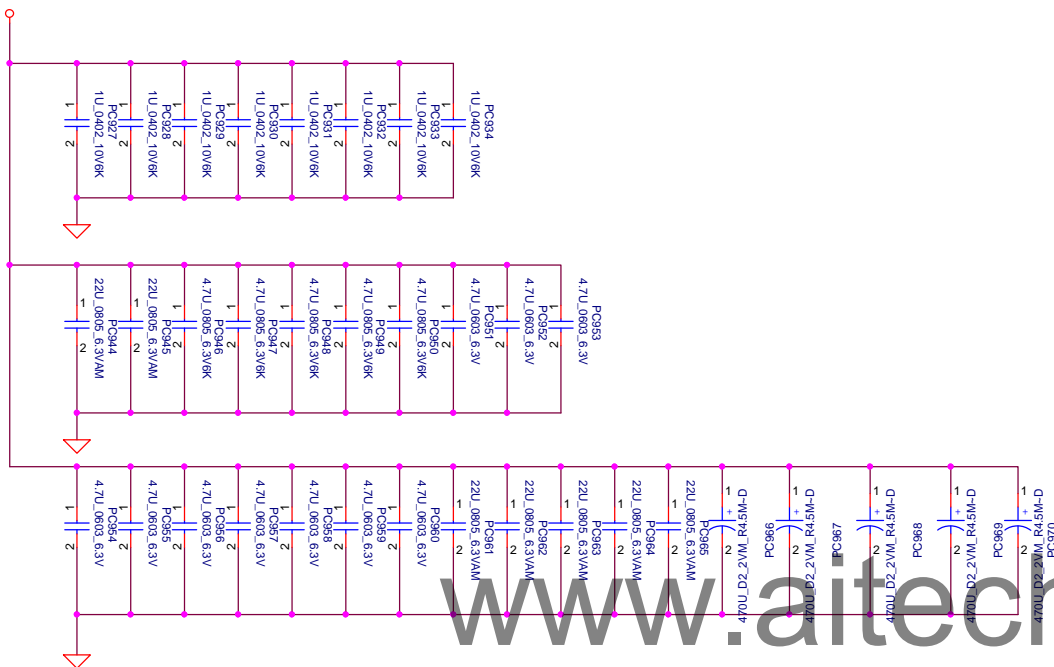
$$V_{out} = 0.8V * (1 + R_{up}/R_{down})$$

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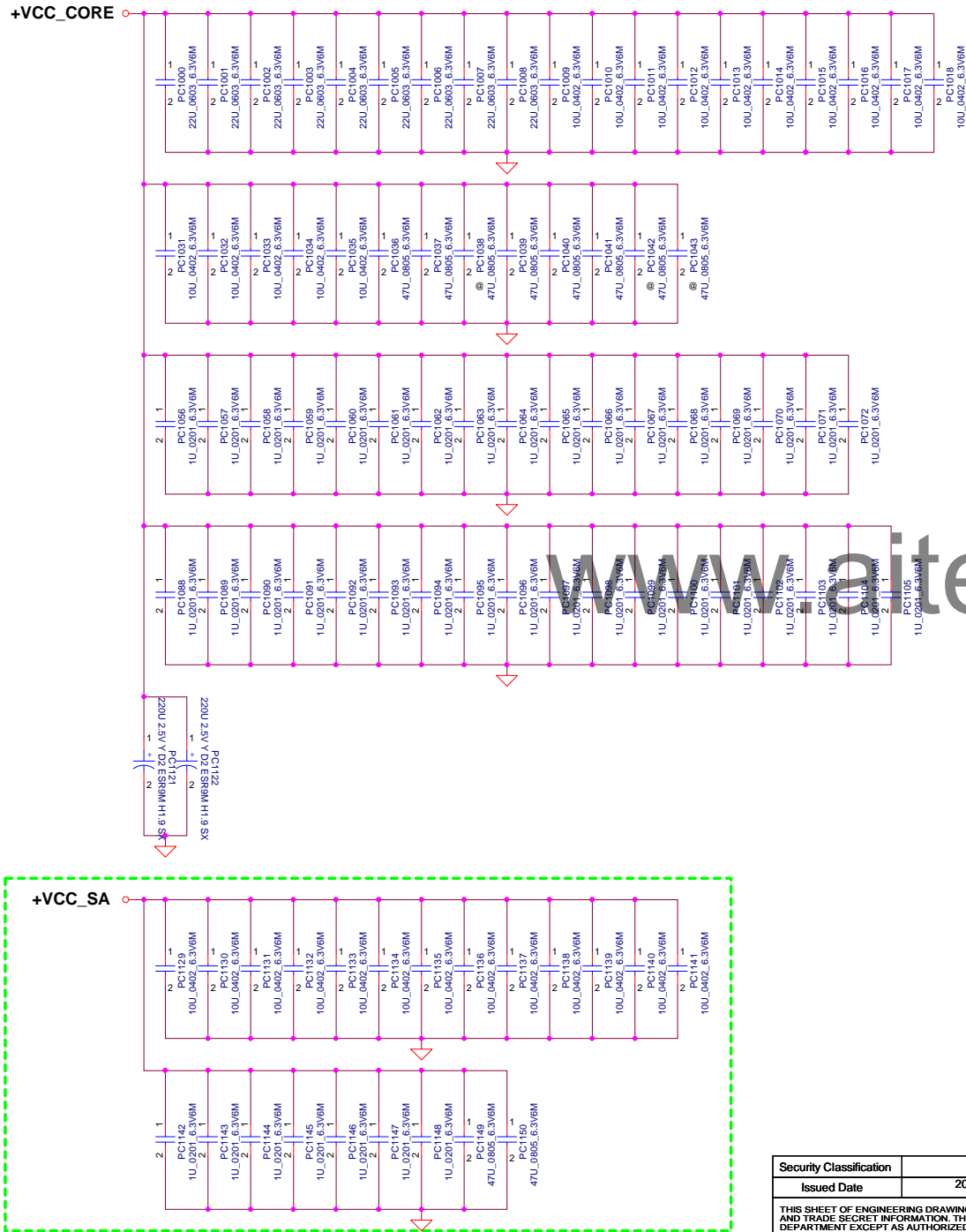


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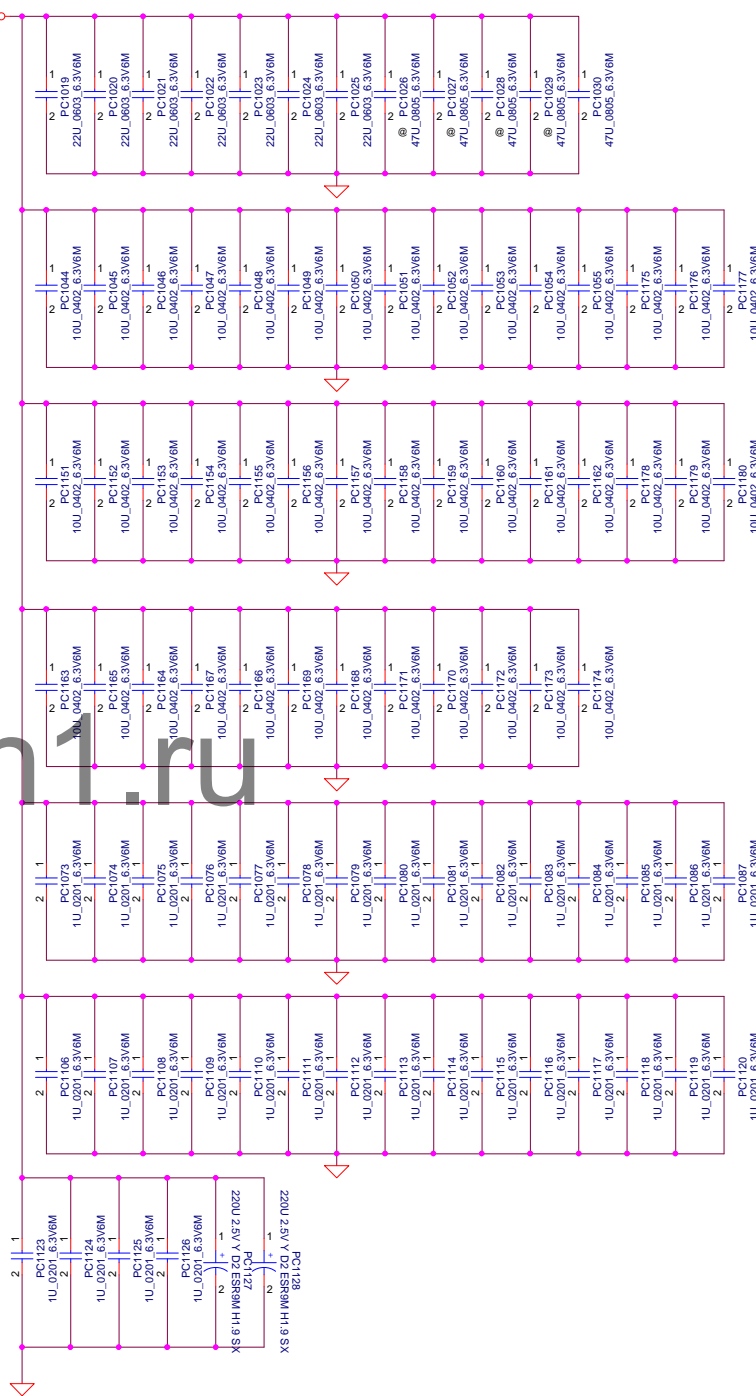
+VGA_CORE



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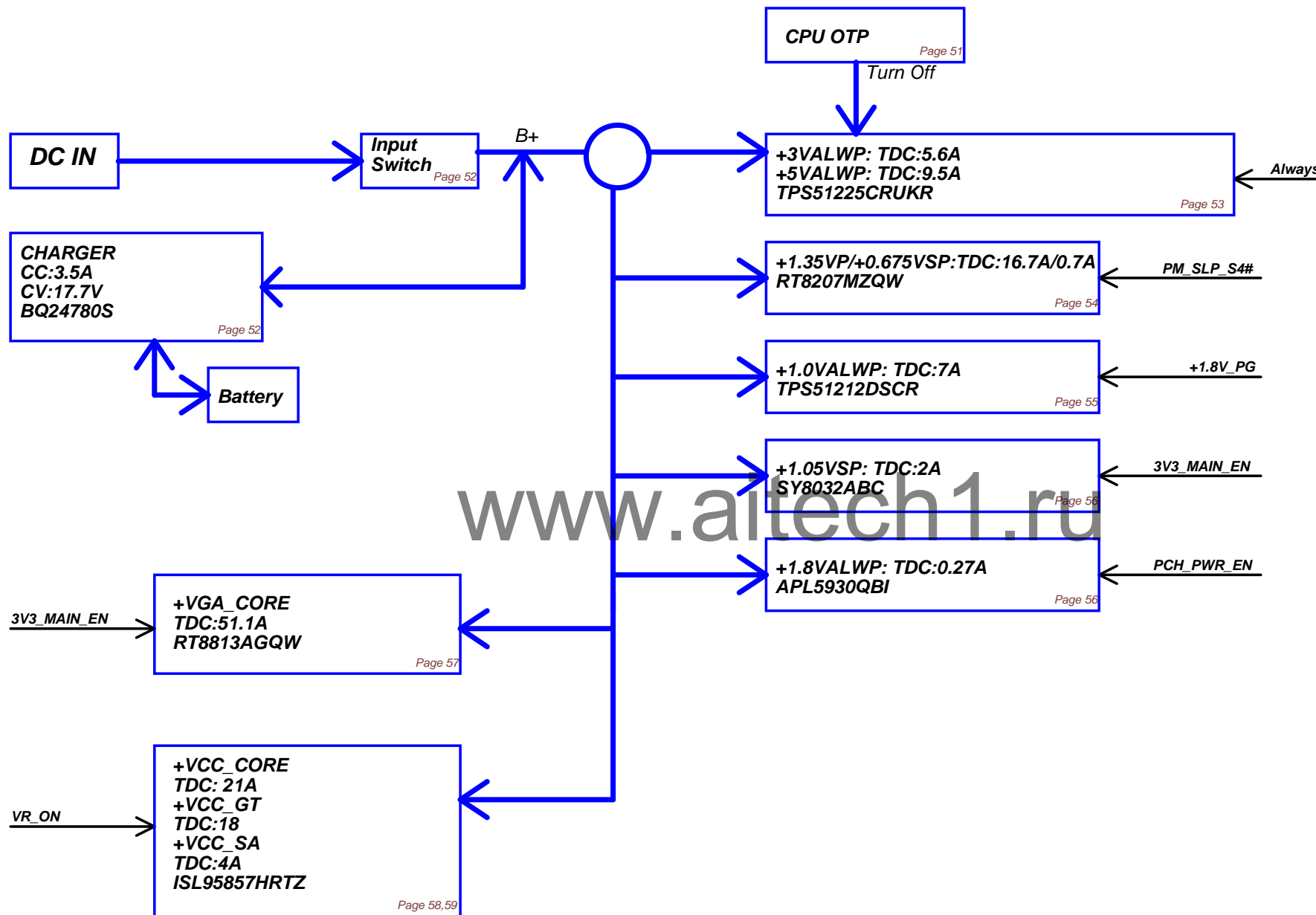


+VCC_GT



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Power block



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Version Change List (P. I. R. List)

Page 1

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	56	1.05VS_VGA	2015/3/6	Compal_PWR	For EE request to fine tune power sequence.	Change PR812 from 33k to 62k.	X01
2	57	VGA_CORE	2015/3/6	Compal_PWR	For EE request to fine tune power sequence.	Change PR615 from 33k to 0. Non-pop PC618.	X01
3	58,59	CPU	2015/4/1	Compal_PWR	For CPU transient and DC/DC EA fine tune.	Change PR550 from 2kOhm to @. Change PC547 from 680pF to @. Change PC543 from 0.01uF to @. Change PC527 from 0.01uF to @. Change PR552 from 2.61kOhm to 4.42kOhm. Change PR529 from 2.61kOhm to 4.42kOhm. Change PC516 from 2200pF to 1000pF. Change PR570 from @ to 20MOhm. Change PR553,PR564 from 2.2 to 4.7ohm	X01
4	54	1.35VP	2015/4/7	Compal_PWR	For EE request to fine tune power sequence.	Add PR210 to connect with PM_SLP_S4# , non-pop PR208.	X01
5	54	1.35VP	2015/4/8	Compal_PWR	For fine tune OCP.	Change PR201 from 8.06kohm to 10kom.	X01
6	55	1.0VALWP	2015/4/8	Compal_PWR	Improve output ripple voltage.	Add PC307.	X01
7	51	DCIN/BATT CONN/OTP	2015/5/20	Compal_PWR	For change CPU OTP point	Change PR24 from 12.1k to 16.2k.	X04
8	51	DCIN/BATT CONN/OTP	2015/7/8	Compal_PWR	For cost down removed baed	remove PL1,PL2,PL3	1.0
9	57	VGA_CORE	2015/7/8	Compal_PWR	For cost down change baed to jumper	Add PJ600	
10	53	3.3VALWP	2015/7/8	Compal_PWR	For cost down removed baed	remove PL101	
11	56	1.8V_PRIM	2015/7/8	Compal_PWR	HW didn't need this. remove PR811	remove PR811	1.0 1.0

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